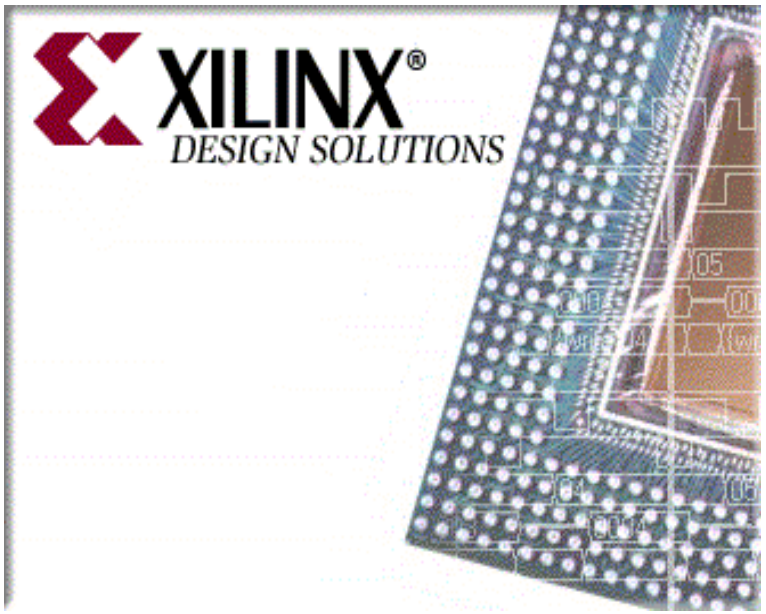
Evaluation of a Design Flow for exploiting Partial Reconfiguration

TECHNISCHE UNIVERSITÄT DARMSTADT

Bachelorarbeit Präsentation

Eingebettete Systeme und ihre Anwendungen
Prof. Dr. Andreas Koch



Übersicht

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- Aufgabenstellung und Motivation
- Derzeitige Situation
- Einblicke in die Partielle Rekonfiguration
- Umsetzung
  - Integrated Software Environment (ISE)
  - PlanAhead
  - Testen
- Ausblick
- Zusammenfassung

Aufgabenstellung

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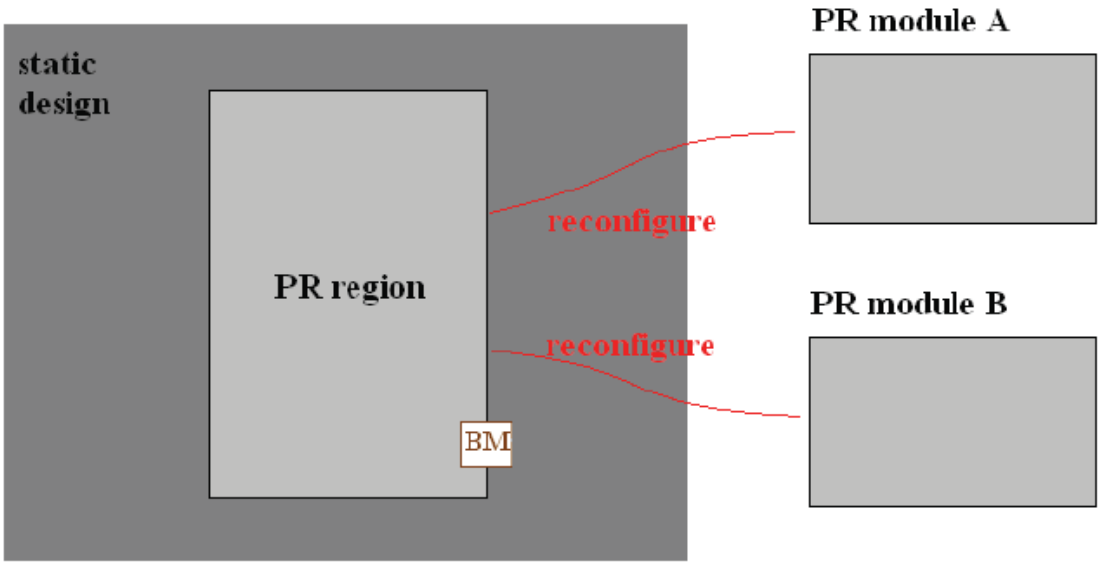
- Teil-Rekonfigurierung eines FPGAs
  - Einarbeitung in Tools
  - Entwicklung
  - Testen
- Up to date
- Zukunft



Derzeitige Situation

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- Häufiger Einsatz von FPGAs
- Programmierung
  - Vollständig
  - Partiell (möglich)
- Probleme
  - Platz
  - Geschwindigkeit
  - Kosten

Einblick in die Partielle Rekonfiguration

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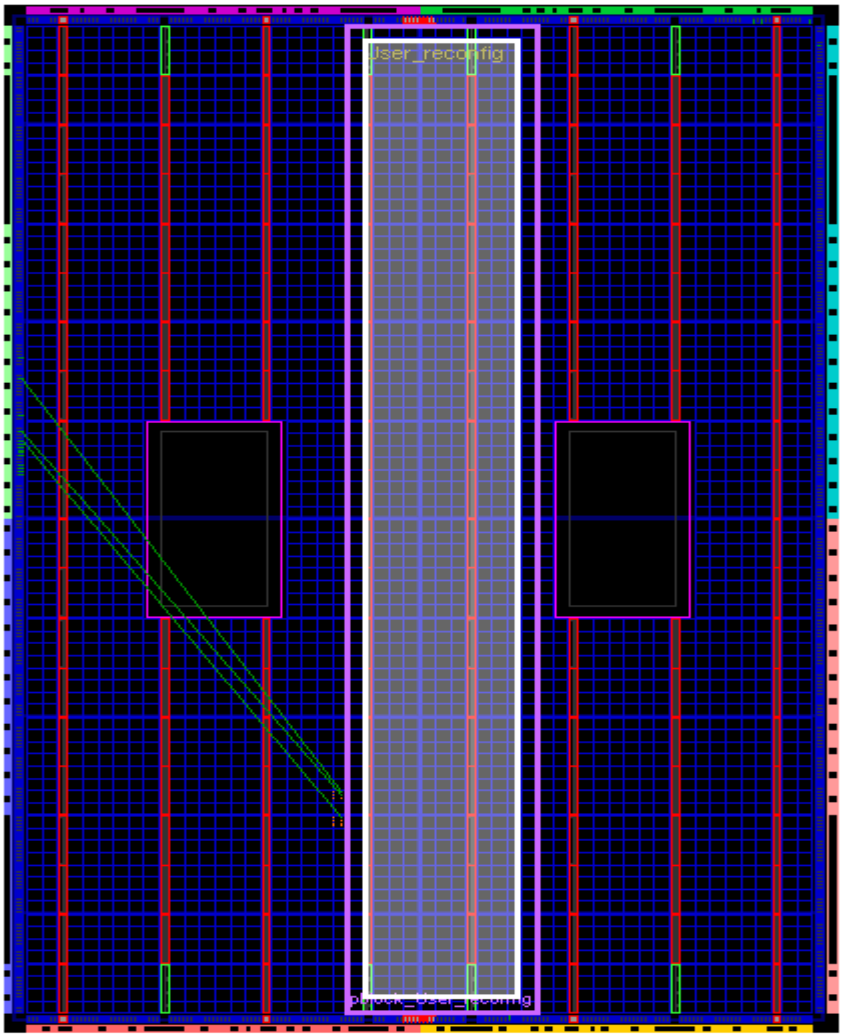
- Möglichkeit seit Virtex 2
- Einfaches System
  - Statisches Design
  - Partielle Region(en)
  - Partielle Module
  - Bus Macros



Bus Macro

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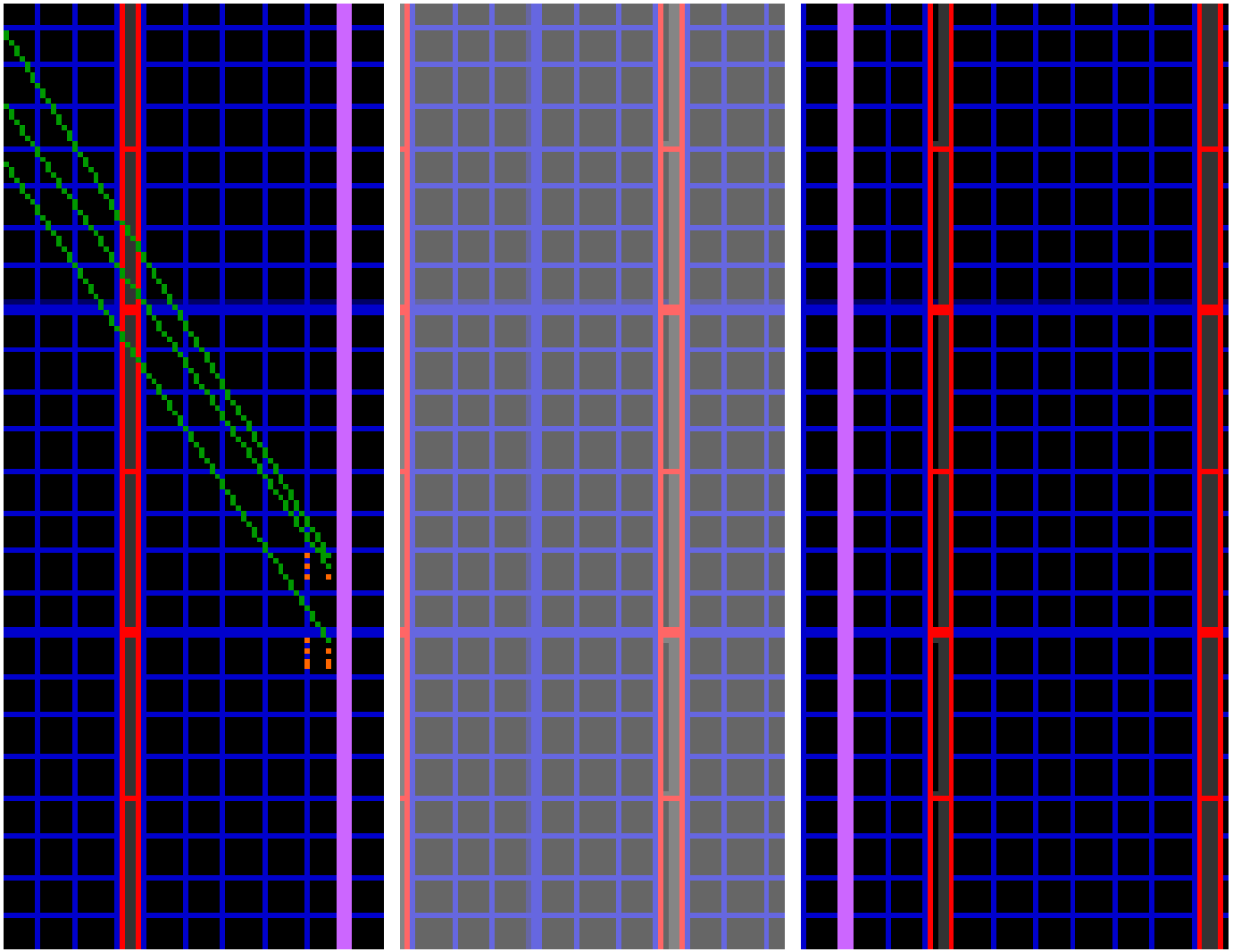

Umsetzung

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- Designentwicklung
- „Place & Route“
- Export des Bitstreams
- Hardware Test

ISE

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- Erstellung der Verilog-Dateien
- Synthetisieren

ISE (fort.)

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- Unterteilung in Module
  - Top
  - Statisch
  - Partiell

Top Level

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- Black Boxes
- Instantiierung (Verbindungen)

```
        reg[7:0] topOut;                // register for the LED output
        wire[7:0] reconfig_Bus_out;     // the output of the Busmacro
        wire[7:0] reconfig_out;         // the reconfig area output
        wire[7:0] static_out;           // the output from the static module
```

```
// instantiate reconfigurable module
reconfig User_reconfig
        (
                .clk        (clk),
         .out   (reconfig_out)
        );
```

```
module static (clk, in, out);

  input clk; // 100MHz input clock
  input[7:0] in; // Input from the PR
  output[7:0] out; // Output to the top
endmodule
```

```
module reconfig (clk, out);

   input  clk;  // 100 MHz input clock
   output[7:0] out; // Output of the PR
       region
endmodule
```

Statisches Projekt

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- Festes Design
- Nicht partiell rekonfigurierbar
- Speichermanagment

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    11:18:55 11/11/2007
// Design Name:
// Module Name:    static
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module static(clk, in, out);
    input clk;
    input [7:0] in;
    output [7:0] out;
        reg[7:0] out;
        always @(posedge clk) begin
         out = in;
        end
        marc marcmodule(clk, in);

endmodule
```

Partiell rekonfigurierbar

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- Module für die PR

```
// module for the right light wave
module reconfig (
      clk,
      out
      );

 input   clk;    // 100 MHz input clock
 output[7:0] out;
 reg [7:0] out2;
 reg[32:0] counter;
 reg[1:0] start;

 assign out = out2;

 always @(posedge clk) begin
  out2[0] <= 0;
        out2[1] <= 1;
        if (counter == 'd16777216) begin
         out2[2] <= (start == 'b11)?1:0;
         out2[3] <= out2[2];
         out2[4] <= out2[3];
         out2[5] <= out2[4];
         out2[6] <= out2[5];
         out2[7] <= out2[6];
         counter <= 'b0;
         start <= start+1;
        end
        else begin
         counter <= counter + 1;
        end
end

endmodule
```

```
// module for the left light wave
module reconfig (
      clk,
      out
      );

 input   clk;    // 100 MHz input clock
 output[7:0] out;
 reg [7:0] out2;
 reg[32:0] counter;
 reg[1:0] start;

 assign out = out2;

 always @(posedge clk) begin
  out2[0] <= 1;
        out2[1] <= 0;
        if (counter == 'd16777216) begin
         out2[7] <= (start == 'b11)?1:0;
         out2[6] <= out2[7];
         out2[5] <= out2[6];
         out2[4] <= out2[5];
         out2[3] <= out2[4];
         out2[2] <= out2[3];
         counter <= 'b0;
         start <= start+1;
        end
        else begin
         counter <= counter + 1;
        end
end

endmodule
```

Synthetisieren

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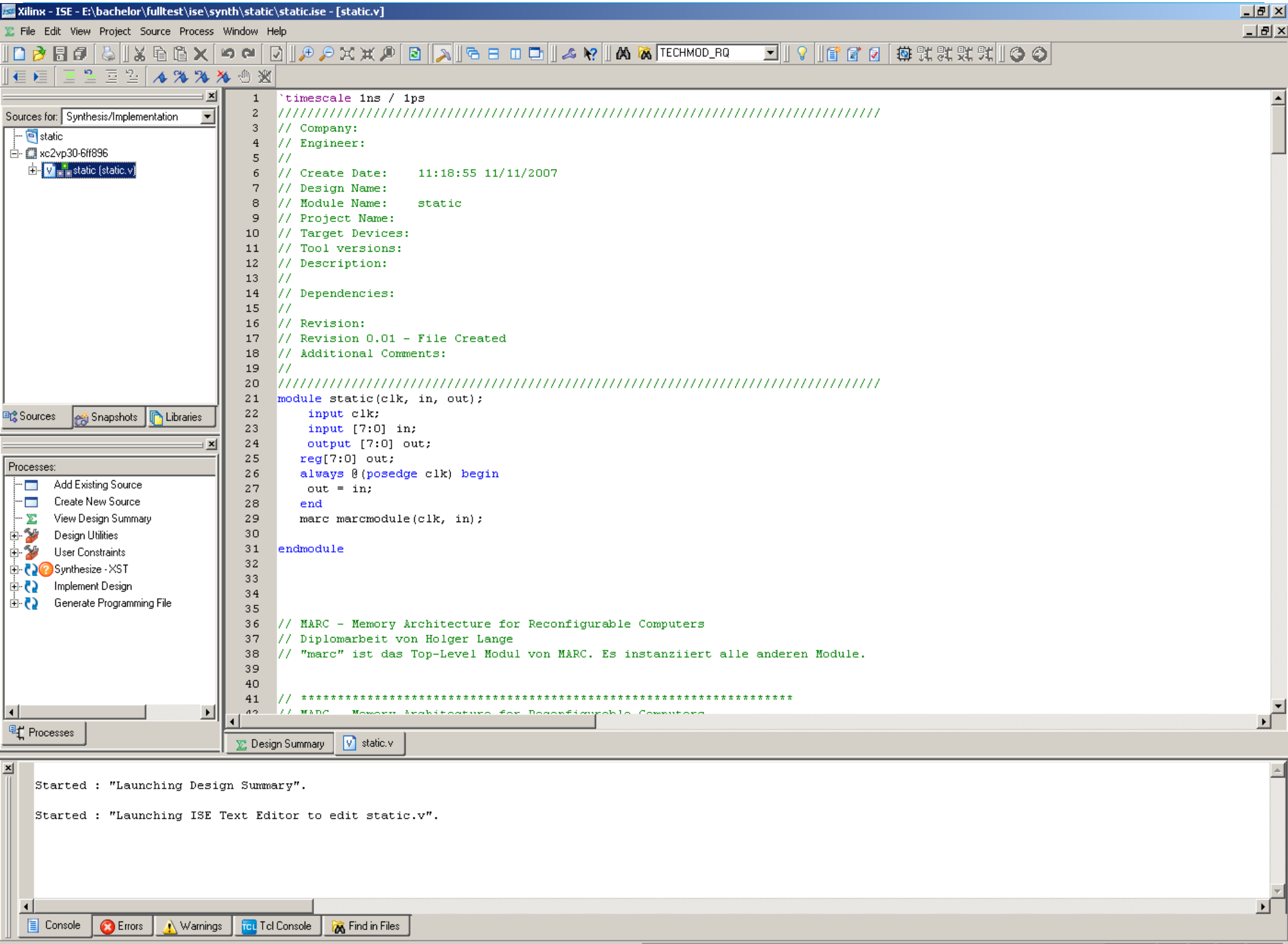
- Logisches Design und Constraints
- Bsp: top.ngc
  - Umwandlung zu *ndf*


Xilinx - ISE - E:\bachelor\fulltest\ise\synth\static\static.ise - [static.v]
File Edit View Project Source Process Window Help
TECHMOD_RQ
Sources for: Synthesis/Implementation
static
xc2vp30-6ff896
static (static.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Processes
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 11:18:55 11/11/2007
7 // Design Name:
8 // Module Name: static
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module static(clk, in, out);
22 input clk;
23 input [7:0] in;
24 output [7:0] out;
25 reg[7:0] out;
26 always @(posedge clk) begin
27 out = in;
28 end
29 marc marcmodule(clk, in);
30
31 endmodule
32
33
34
35
36 // MARC - Memory Architecture for Reconfigurable Computers
37 // Diplomarbeit von Holger Lange
38 // "marc" ist das Top-Level Modul von MARC. Es instanziiert alle anderen Module.
39
40
41 // ***
Design Summary
static.v
Started : "Launching Design Summary".
Started : "Launching ISE Text Editor to edit static.v".
Console
Errors
Warnings
Tcl Console
Find in Files

PlanAhead

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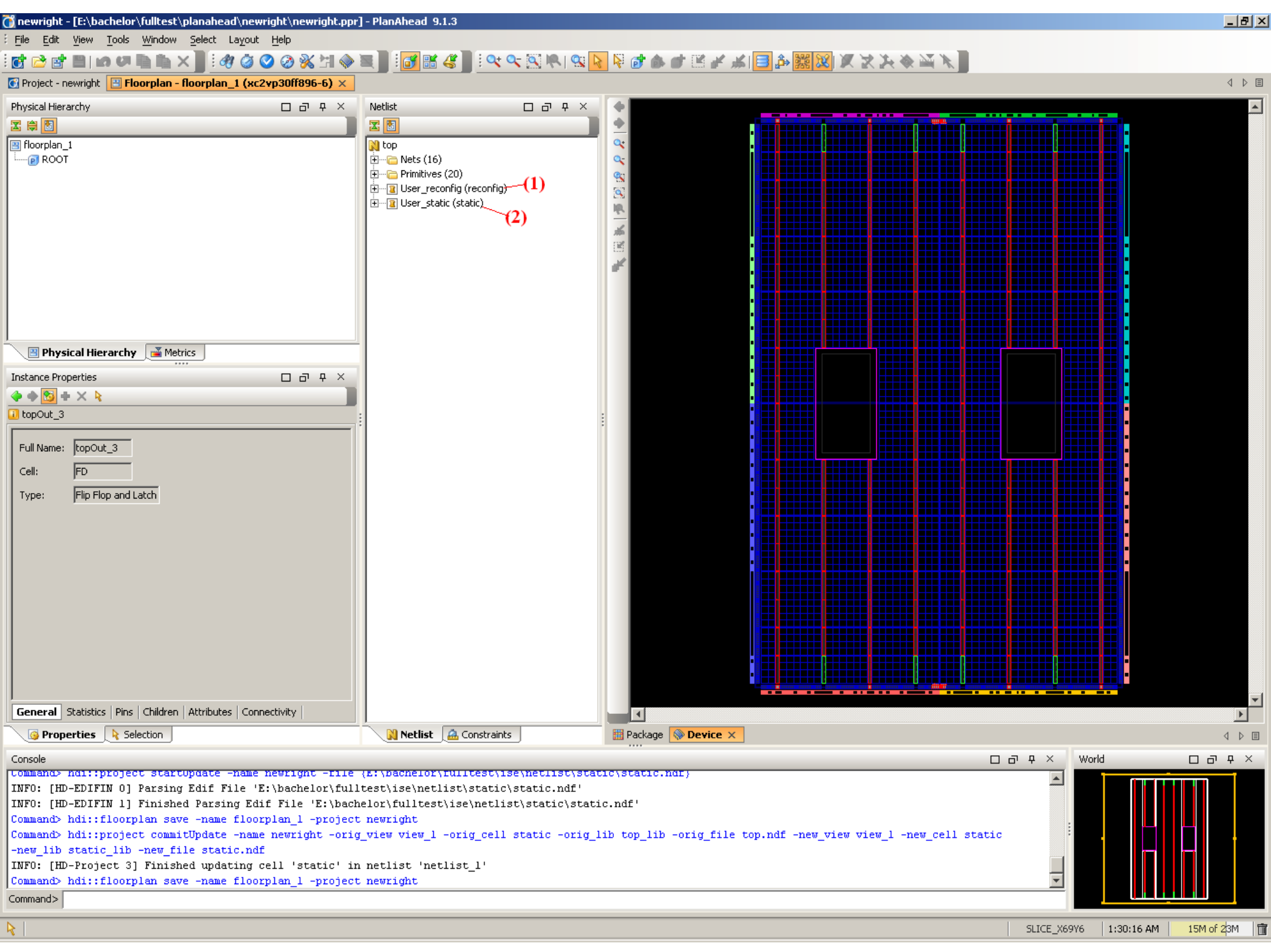
- Platzierung der synthetisierten Module
  - Inkl. Bus Macros
- Ermöglicht Partielle Rekonfiguration
- Exportieren der Bitstreams


newright - [E:\bachelor\fulltest\planahead\newright\newright.ppr] - PlanAhead 9.1.3
File Edit View Tools Window Select Layout Help
Project - newright
Floorplan - floorplan_1 (xc2vp30ff896-6)
Physical Hierarchy
floorplan_1
ROOT
Physical Hierarchy
Metrics
Instance Properties
topOut_3
Full Name: topOut_3
Cell: FD
Type: Flip Flop and Latch
General
Statistics
Pins
Children
Attributes
Connectivity
Properties
Selection
Netlist
top
Nets (16)
Primitives (20)
User_reconfig (reconfig)
User_static (static)
(1)
(2)
Netlist
Constraints
Package
Device
Console
Command> hdi::project startUpdate -name newright -file {E:\bachelor\fulltest\ise\netlist\static\static.ndf}
INFO: [HD-EDIFIN 0] Parsing Edif File 'E:\bachelor\fulltest\ise\netlist\static\static.ndf'
INFO: [HD-EDIFIN 1] Finished Parsing Edif File 'E:\bachelor\fulltest\ise\netlist\static\static.ndf'
Command> hdi::floorplan save -name floorplan_1 -project newright
Command> hdi::project commitUpdate -name newright -orig_view view_1 -orig_cell static -orig_lib top_lib -orig_file top.ndf -new_view view_1 -new_cell static
-new_lib static_lib -new_file static.ndf
INFO: [HD-Project 3] Finished updating cell 'static' in netlist 'netlist_1'
Command> hdi::floorplan save -name floorplan_1 -project newright
Command>
World
SLICE_X69Y6
1:30:16 AM
15M of 23M

Design importieren

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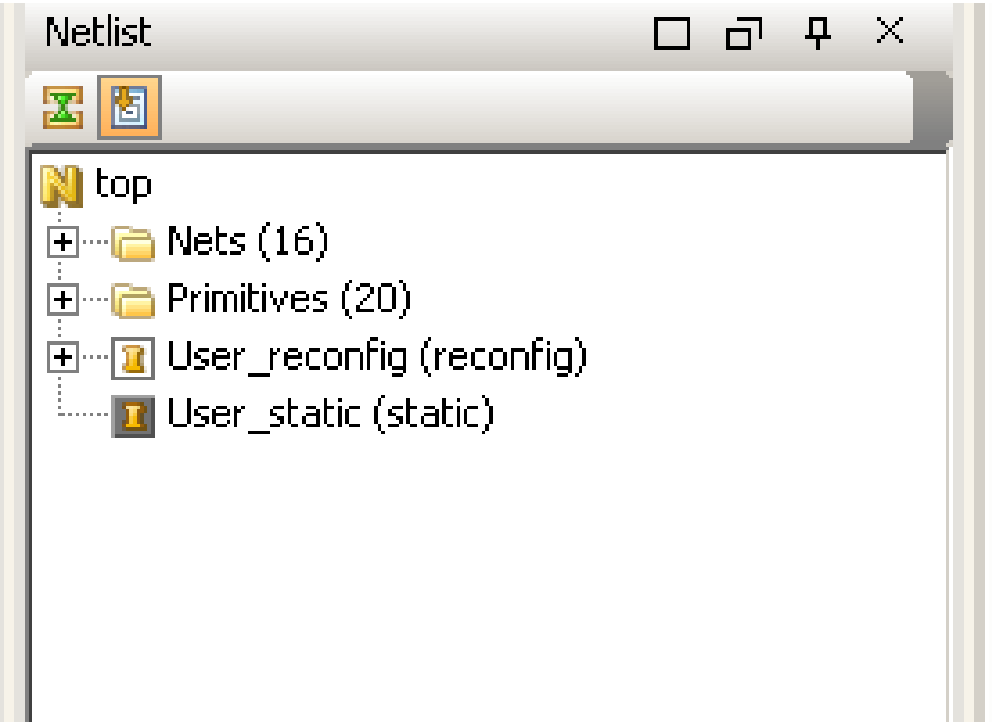
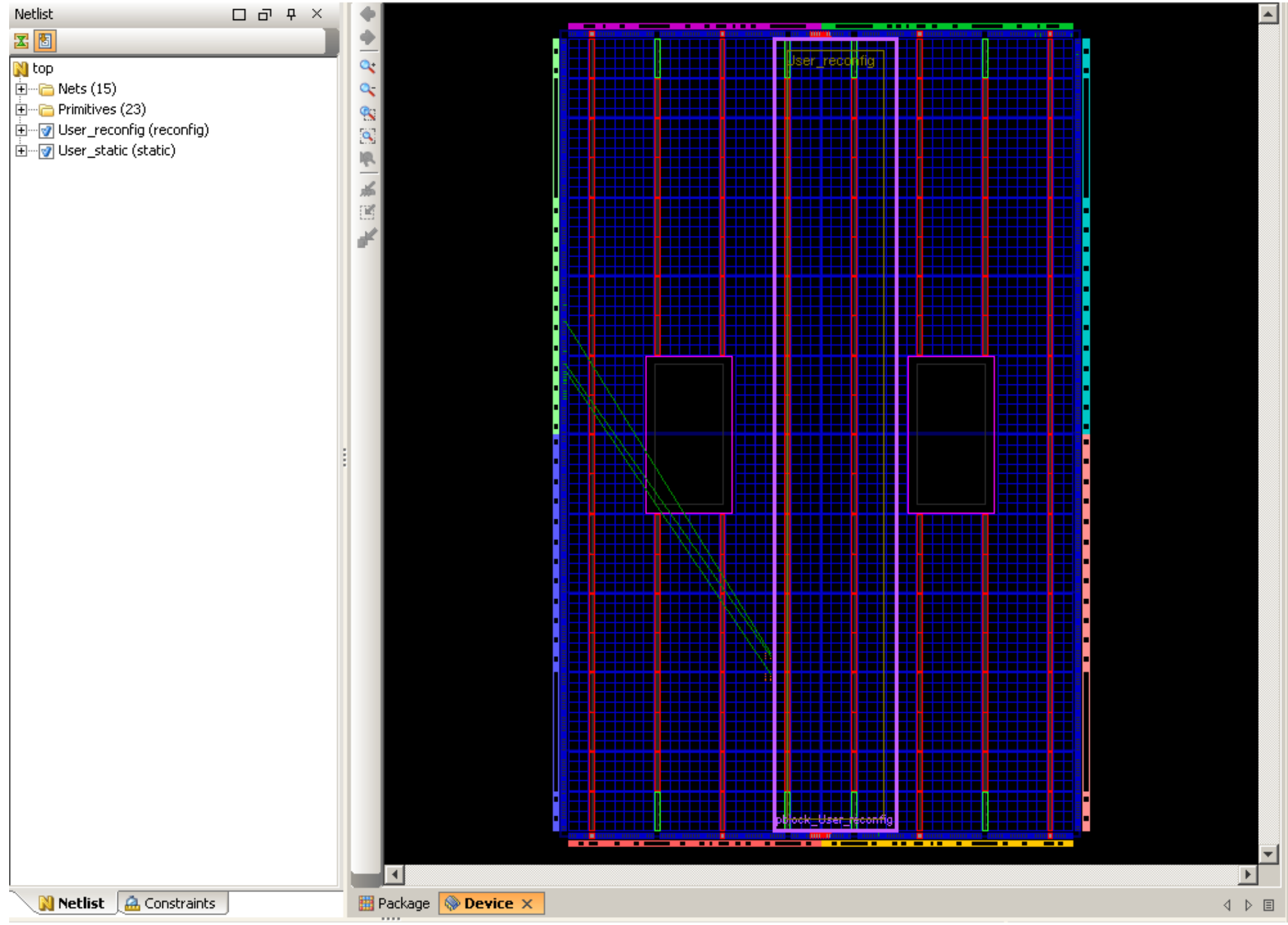
- Logik an das Modul binden
- PR Region platzieren
  - rekonfigurierbar
- Bus Macros platzieren
- Verbinden der Pins




Netlist
top
Nets (15)
Primitives (23)
User_reconfig (reconfig)
User_static (static)
User_reconfig
pblock_User_reconfig
Netlist
Constraints
Package
Device

Abschließen

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- Design Rule Check (DRC)
  - Speziell für PR
- Export der Bitstreams
  - 4 Schritte
- Wiederholen für jede PR

Exportierte Bitstreams

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- Statisches Design
- PR
- Leere PR

static_full.bit
pblock_user_reconfig_cv_routed_partial.bit
pblock_user_reconfig_blank.bit

Testen

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- iMPACT
- Einladen der Bitstreams
- Rekonfigurieren

Ergebnisse

- Vollständig

  vs.

- Partiell

```
// *** BATCH CMD : Program -p 2 -defaultVersion 0
Maximum TCK operating frequency for this device chain: 16700000.
Validating chain...
Boundary-scan chain validated successfully.
'2': Programming device...
PROGRESS_START - Starting Operation.
done.
'2': Reading status register contents...
CRC error                                          :          0
Decryptor security set                             :          0
DCM locked                                         :          1
DCI matched                                        :          1
legacy input error                                 :          0
status of GTS_CFG_B                                :          1
status of GWE                                      :          1
status of GHIGH                                    :          1
value of MODE pin M0                               :          1
value of MODE pin M1                               :          1
value of MODE pin M2                               :          1
value of CFG_RDY (INIT_B)                          :          1
DONEIN input from DONE pin                         :          1
IDCODE not validated while trying to write FDRI    :          0
write FDRI issued before or after decrypt operation:           0
Decryptor keys not used in proper sequence         :          0
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 0111 1111 1000 0000 0000 0000 0000
INFO:iMPACT:579 - '2': Completed downloading bit file to device.
INFO:iMPACT - '2': Checking done pin....done.
'2': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =      4 sec.
```

```
value of MODE pin M1                               :          1
value of MODE pin M2                               :          1
value of CFG_RDY (INIT_B)                          :          1
DONEIN input from DONE pin                         :          1
IDCODE not validated while trying to write FDRI    :          0
write FDRI issued before or after decrypt operation:           0
Decryptor keys not used in proper sequence         :          0
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 0111 1111 1000 0000 0000 0000 0000
INFO:iMPACT:579 - '2': Completed downloading bit file to device.
INFO:iMPACT - '2': Checking done pin....done.
'2': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =      1 sec.
```

Ausblick

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- Umsetzung auf Hardware der ESA-Gruppe
- Partielle Funktionen nun einfach erweiterbar
- Unterschiedliche Bus Macros
- Mehrere PR möglich

Zusammenfassung

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- Kinderkrankheiten in CAD-Tools
- Teilweise ungenaue Dokumentation
- Arbeiten unter Linux schwierig
- Einiges an „Know-How” bzw. Einarbeitung nötig
- Aber! (...)

Zusammenfassung (fort.)

TECHNISCHE UNIVERSITÄT DARMSTADT

- FPGAs vorbereitet für Partielle Rekonfiguration
- Sehr gute Ergebnisse
  - Hohes Potential
- Grundgerüst einfach erweiterbar
- Tools verhältnismäßig stabil (unter Windows)
- Dokumentationen und Bespiele folgen

Abschluss

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Vielen Dank für Ihre Aufmerksamkeit!

Quellen

TECHNISCHE UNIVERSITÄT DARMSTADT

- www.xilinx.com