ILP-based Modulo Scheduling for High-level Synthesis

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NEW ZEALAND

Outline

- Introduction to loop pipelining / modulo scheduling

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- Comparison of a novel & two existing approaches

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Canis et al.

state-of-the-art **heuristic**

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- Comparison of a novel & two existing approaches
  - result quality, heuristic vs. exact
  - **time to schedule** - *it's impractical to do exact modulo scheduling, right?*

Modulo SDC Canis et al.	Formulation by **Eichenberger** & Davidson	**Moovac** Oppermann et al.
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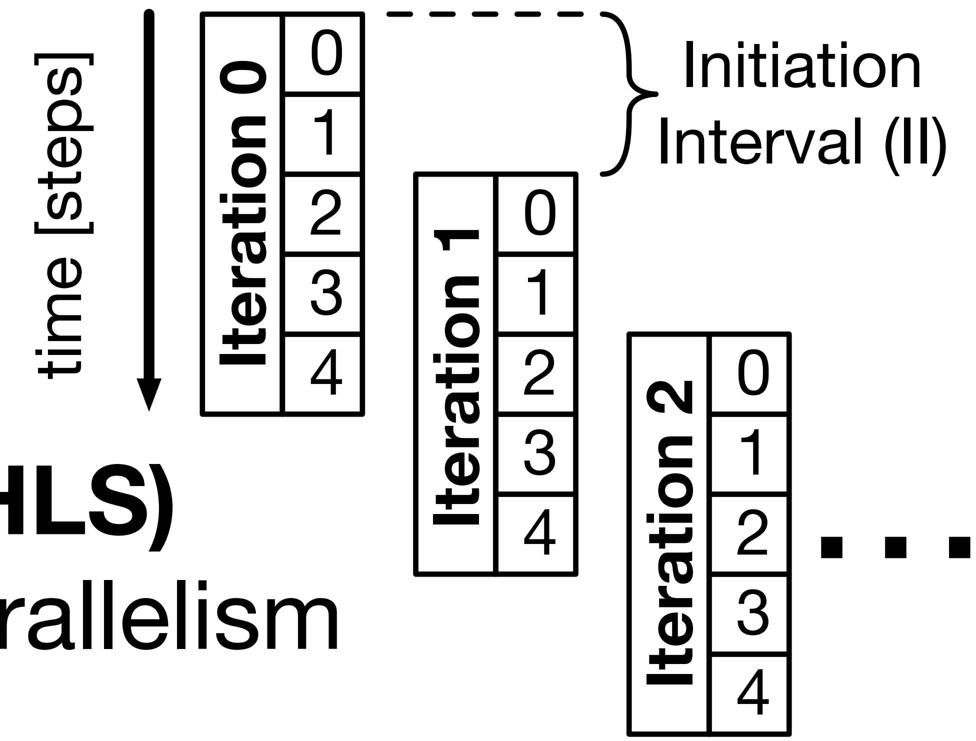
Loop Pipelining

- C-based **High-level Synthesis (HLS)** needs to exploit all sources of parallelism

Loop Pipelining



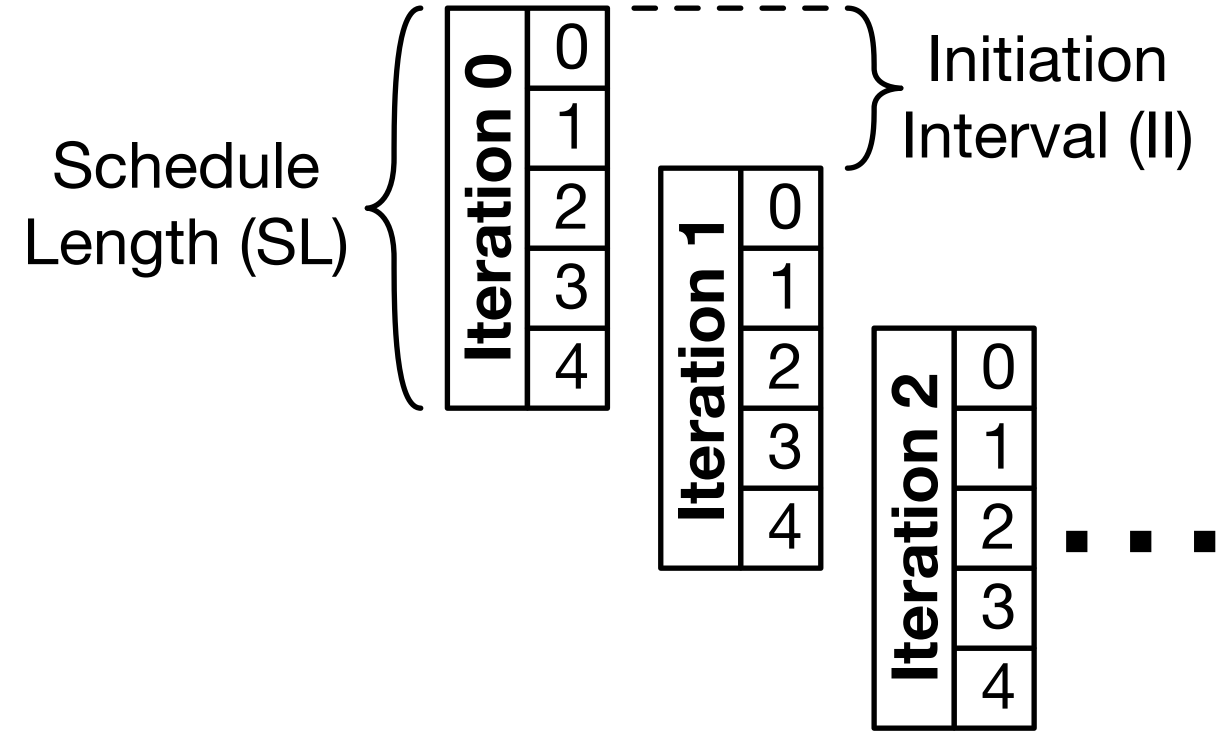
- C-based **High-level Synthesis (HLS)** needs to exploit all sources of parallelism

- **Loop pipelining**
  = new loop iterations are started after a fixed number of time steps, called **Initiation Interval (II)**

  - Partially overlapping execution of subsequent loop iterations

Loop Pipelining

- Increases throughput!



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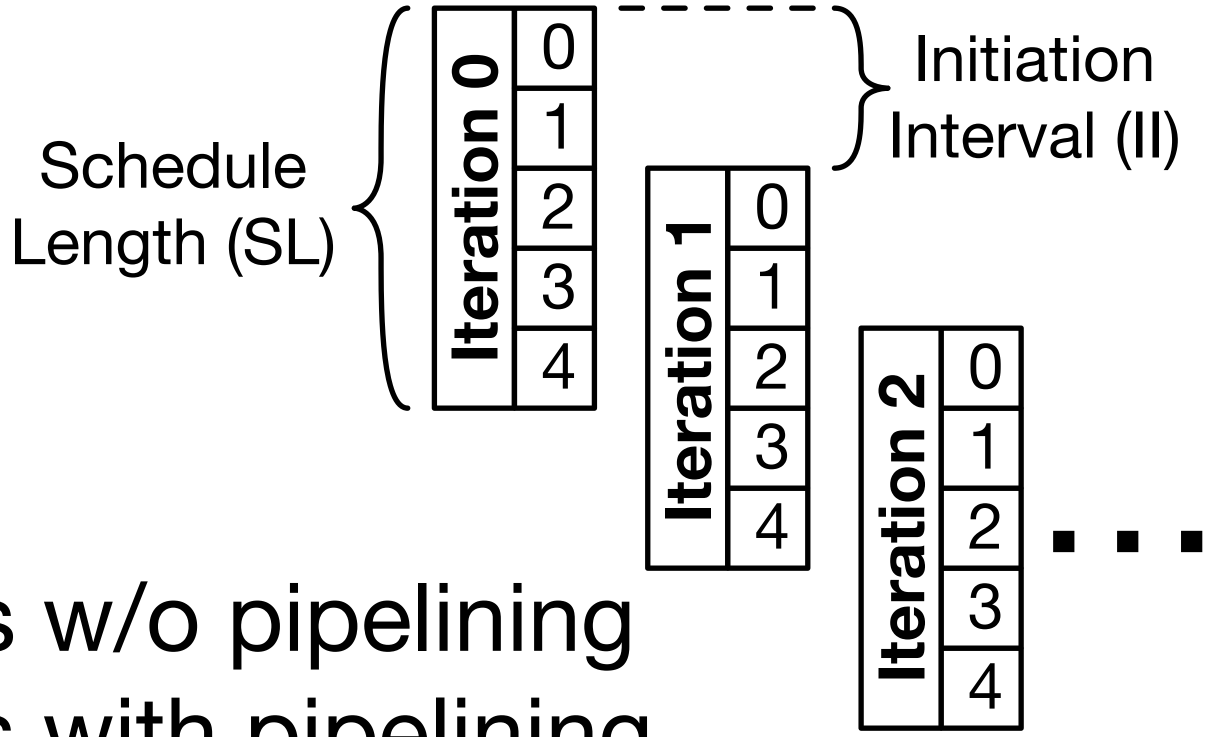

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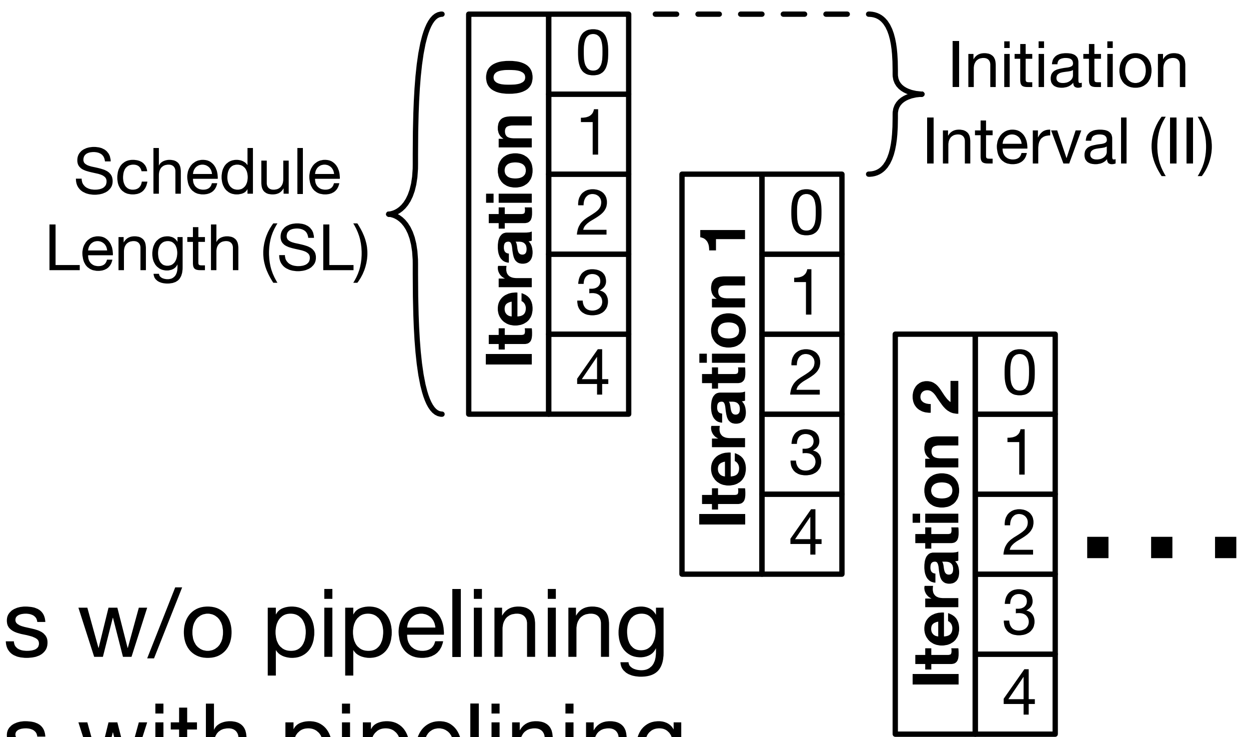
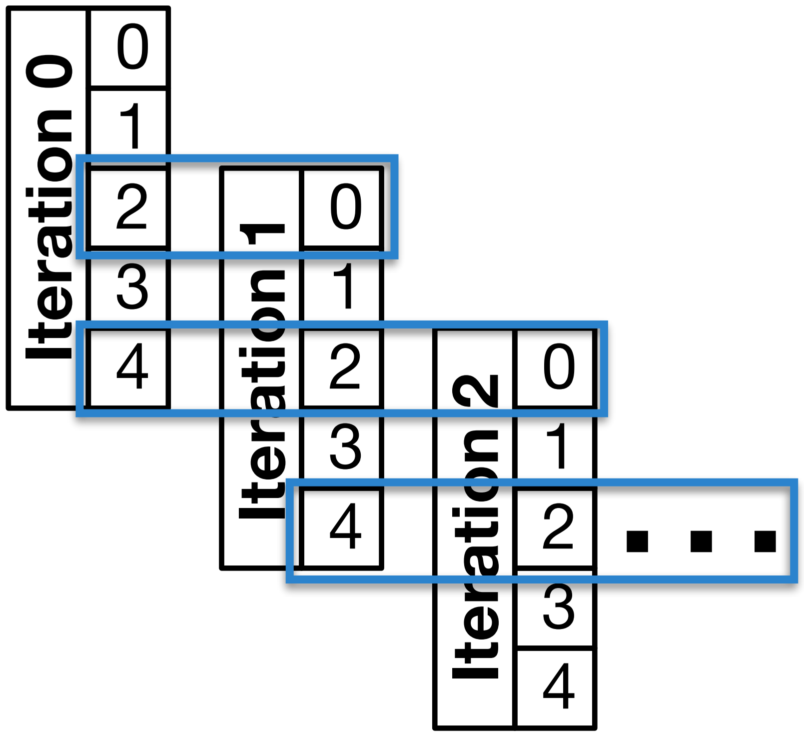


- Increases throughput!
- Executing n iterations →
  $n \cdot SL$ time steps w/o pipelining
  $(n-1) \cdot II + SL$ time steps with pipelining
- Primary objective is to find **smallest feasible II**
  - Limited by dependencies between iterations
  - Subject to resource constraints (cache ports, DSPs, …)

Loop Pipelining

- Operations from different iterations are active at the same time



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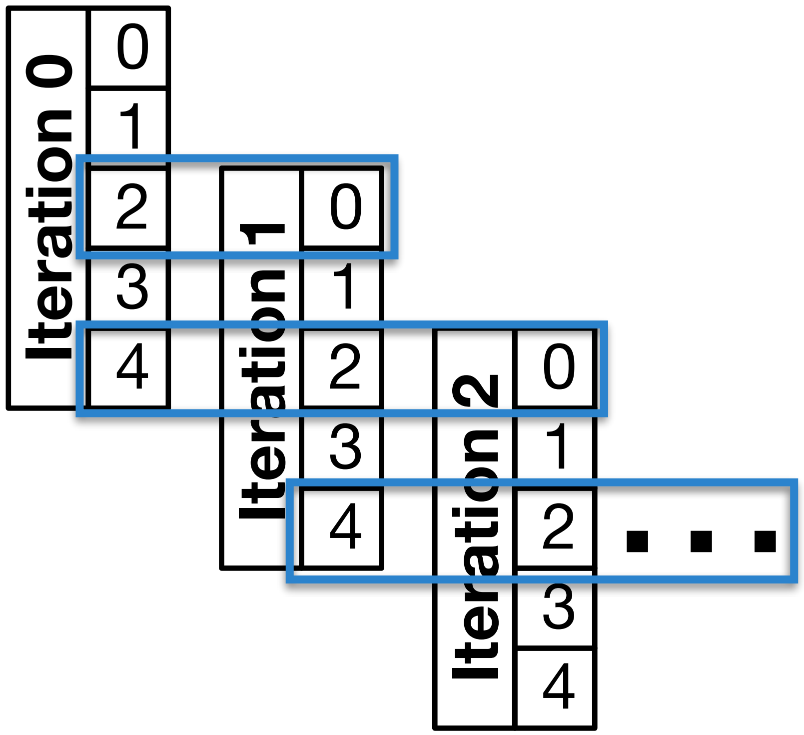

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  - *“modulo resource constraints”*

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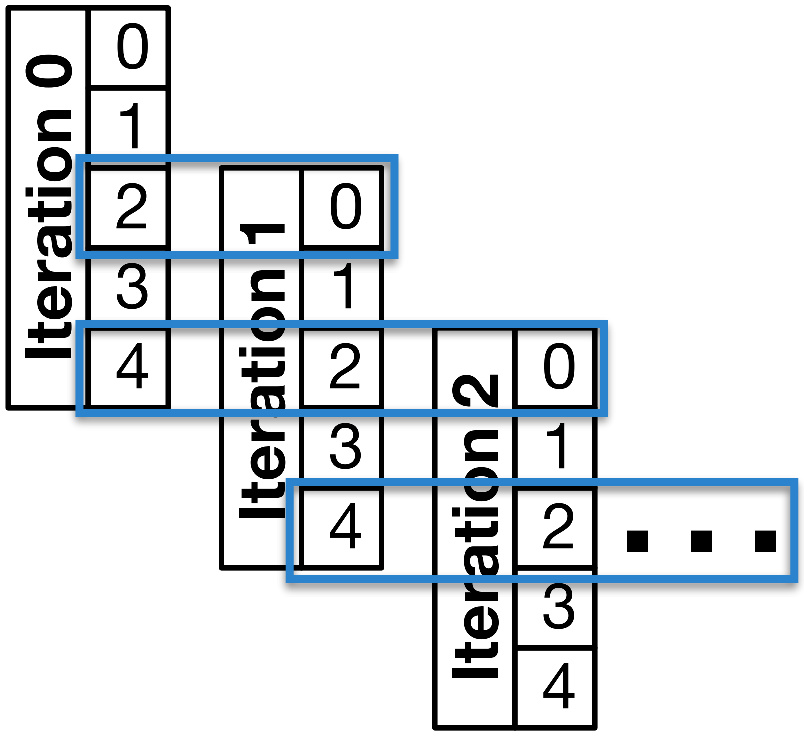

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- Resource constraints have to hold for **congruence classes (modulo II)** of time steps
  - *"modulo resource constraints"*
- Suitable schedules for loop pipelining are found by **modulo schedulers**

Example

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for (i = 1 .. N)
{
  t    = a[i-1];
  a[i] = s + t;
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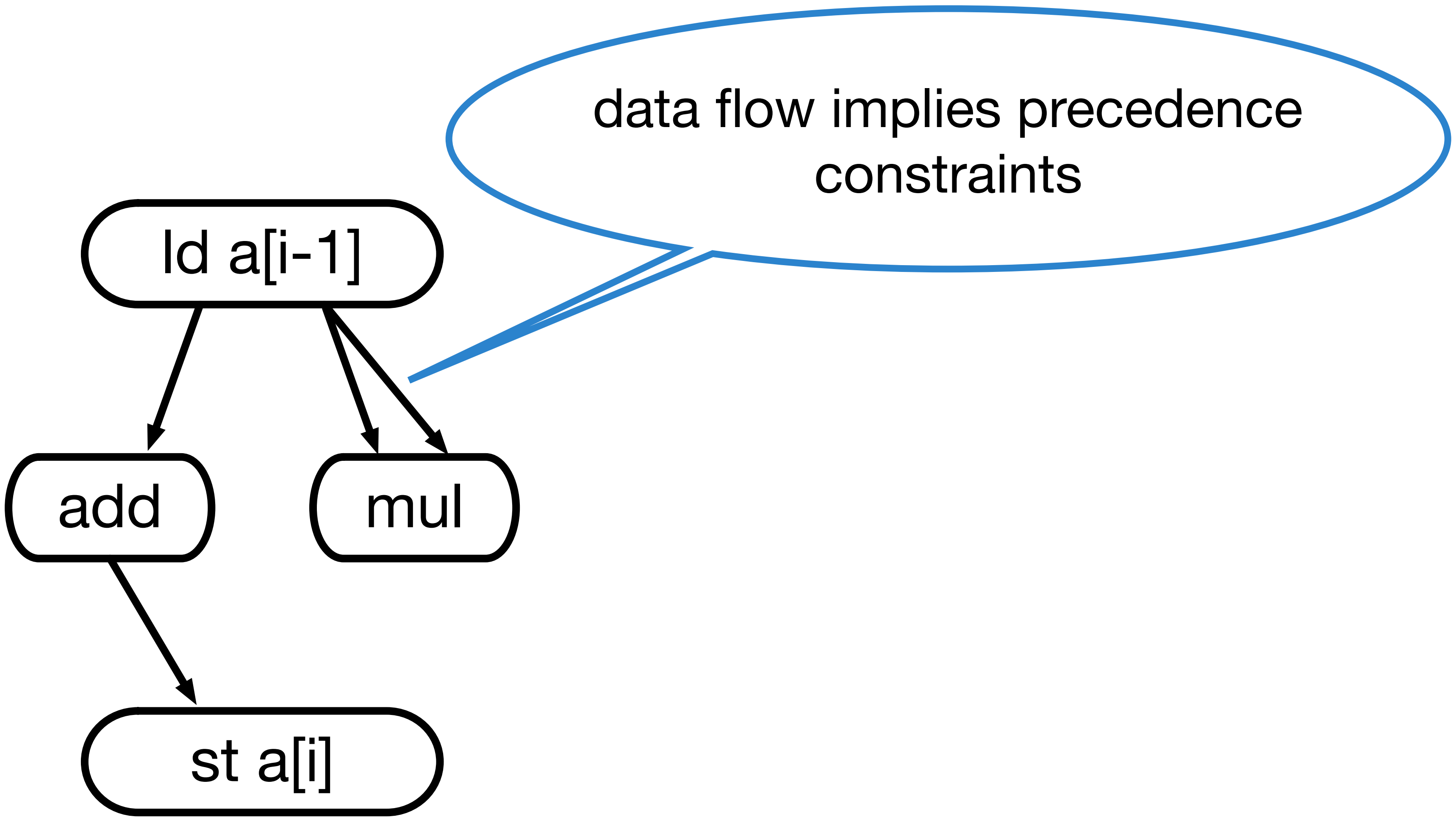

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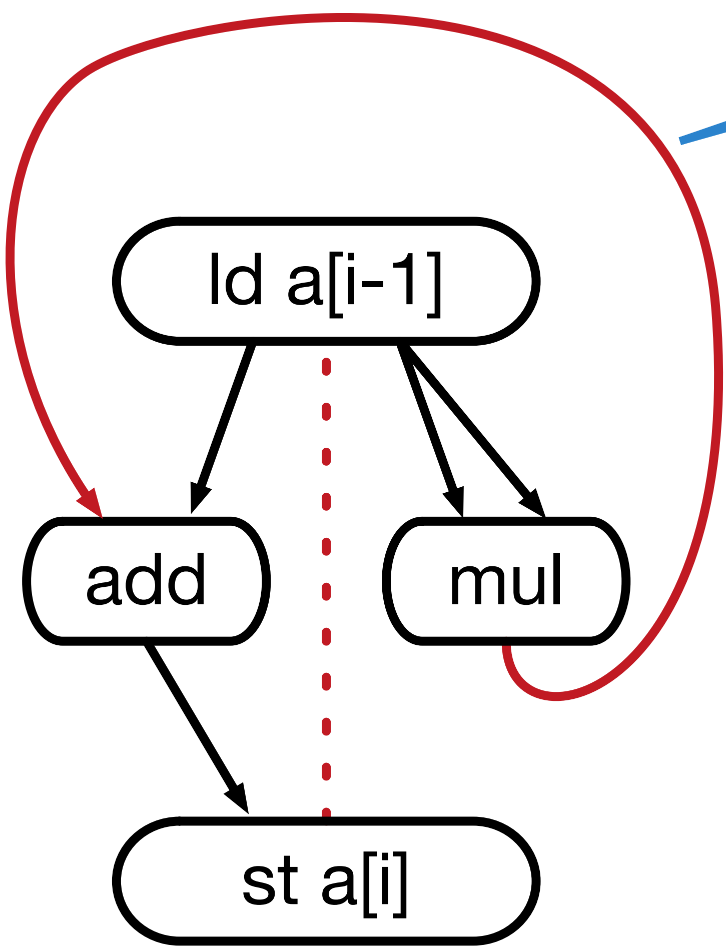

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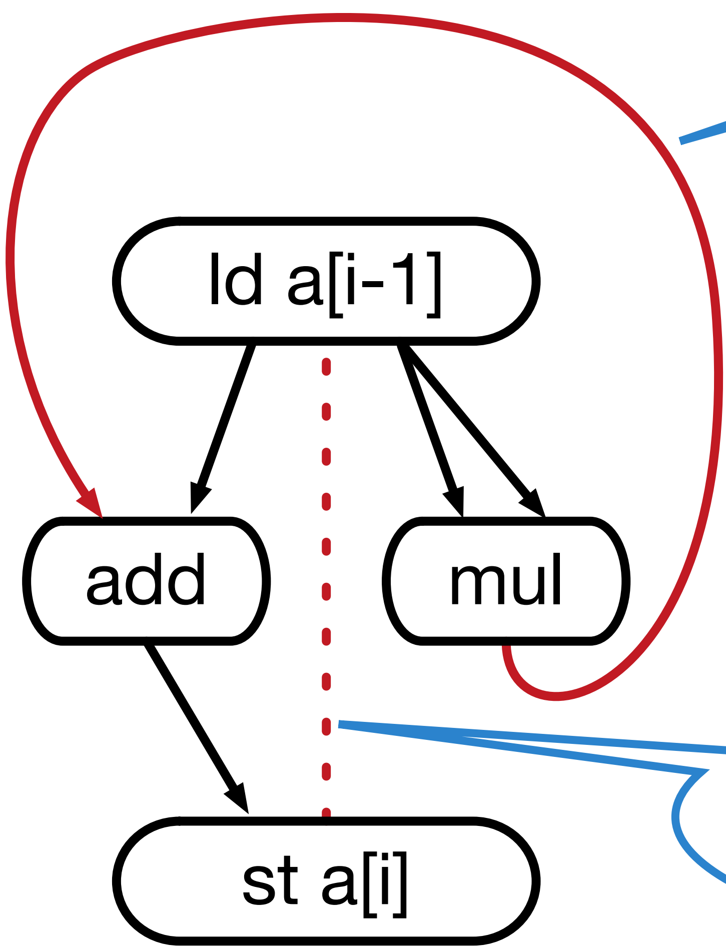

Load value only after it was
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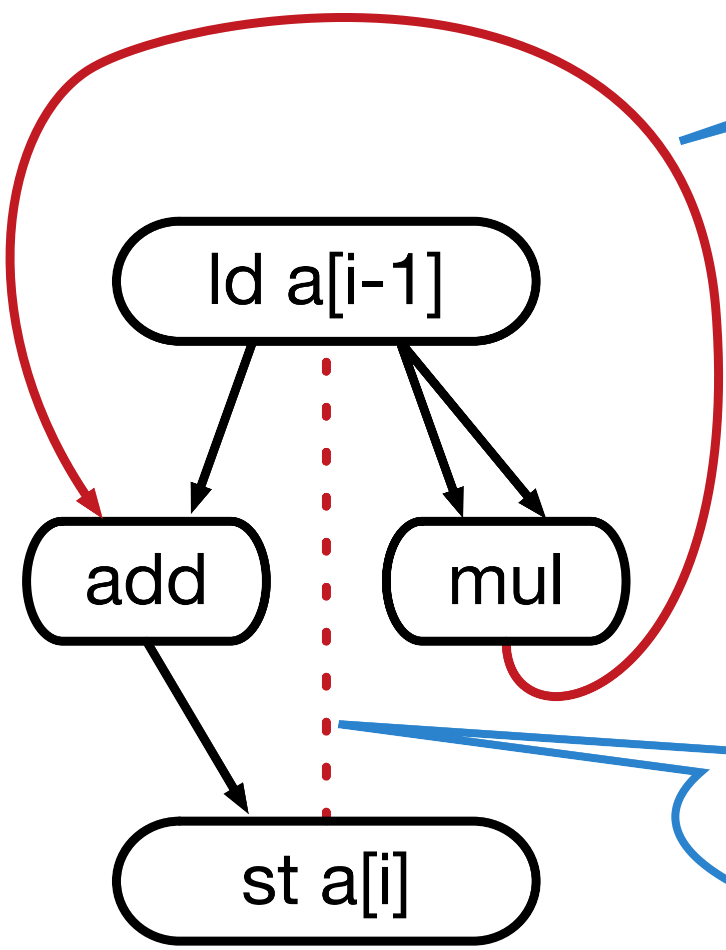

Both edges imply
inter-iteration dependencies
a.k.a “backedges”

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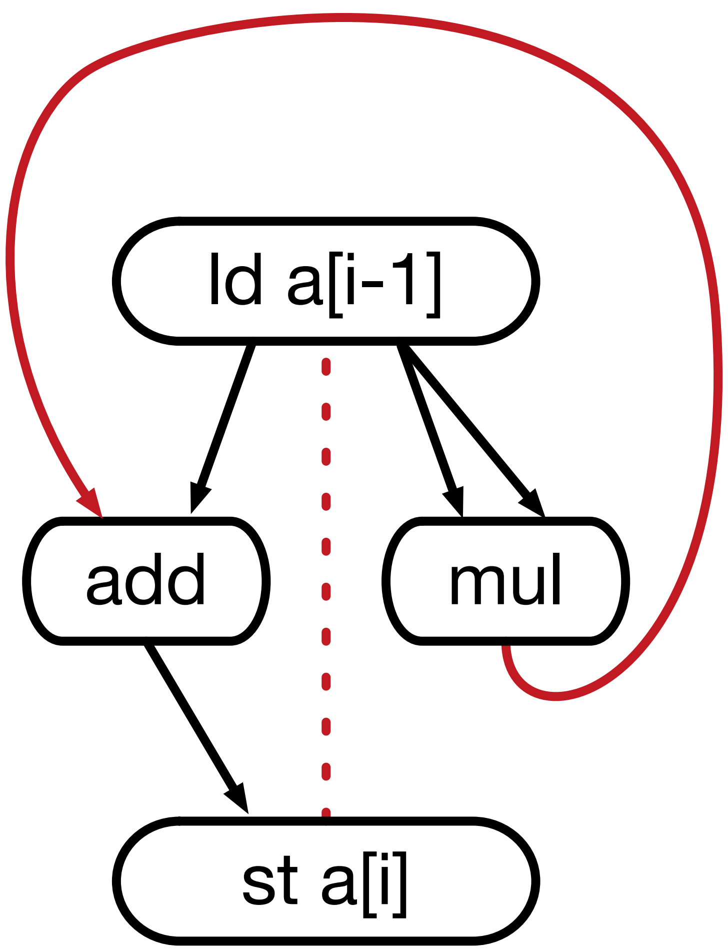

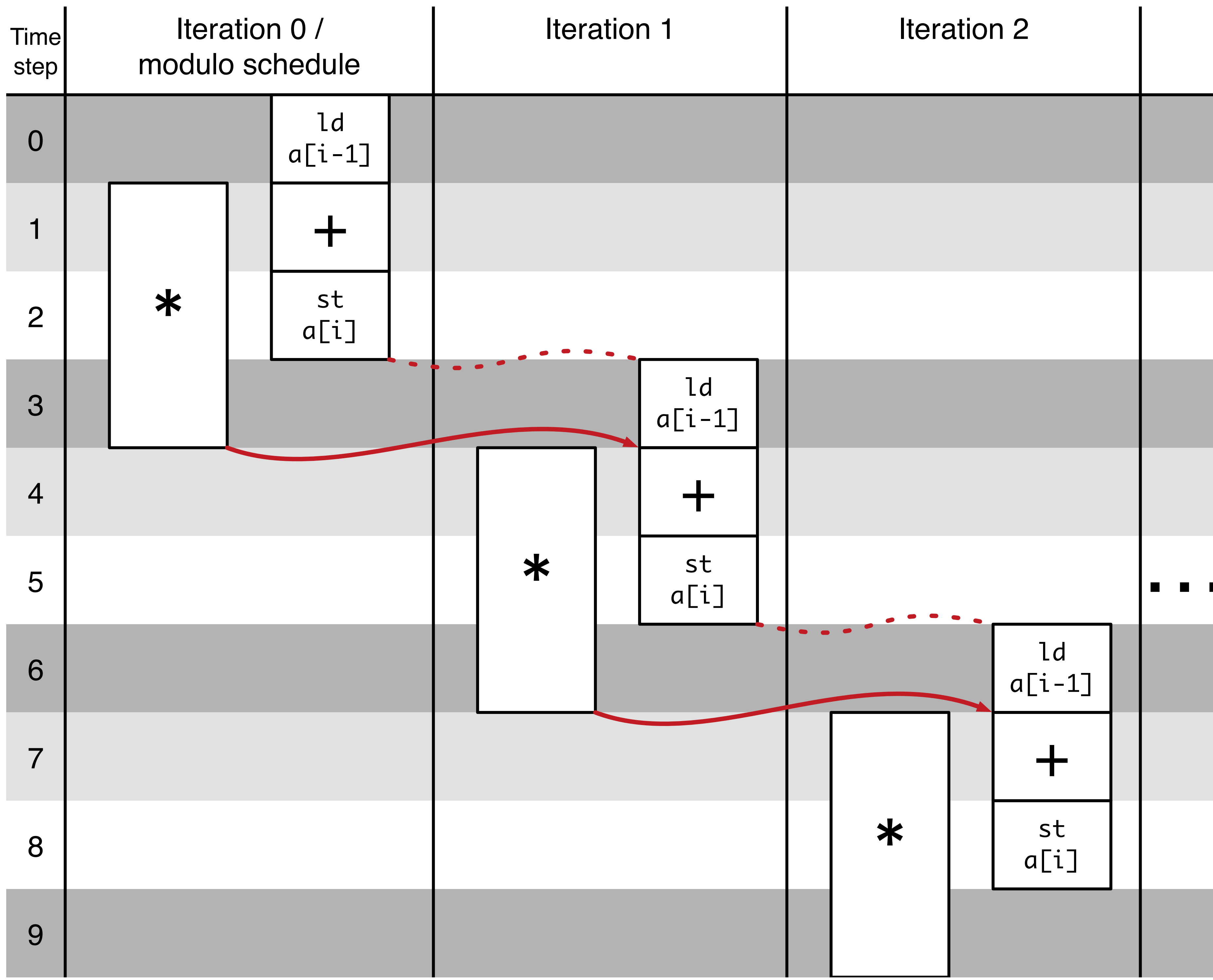

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  - Input: candidate II, precedence edges, resource constraints, operation latencies
  - Output: start times for operations, or attempt fails

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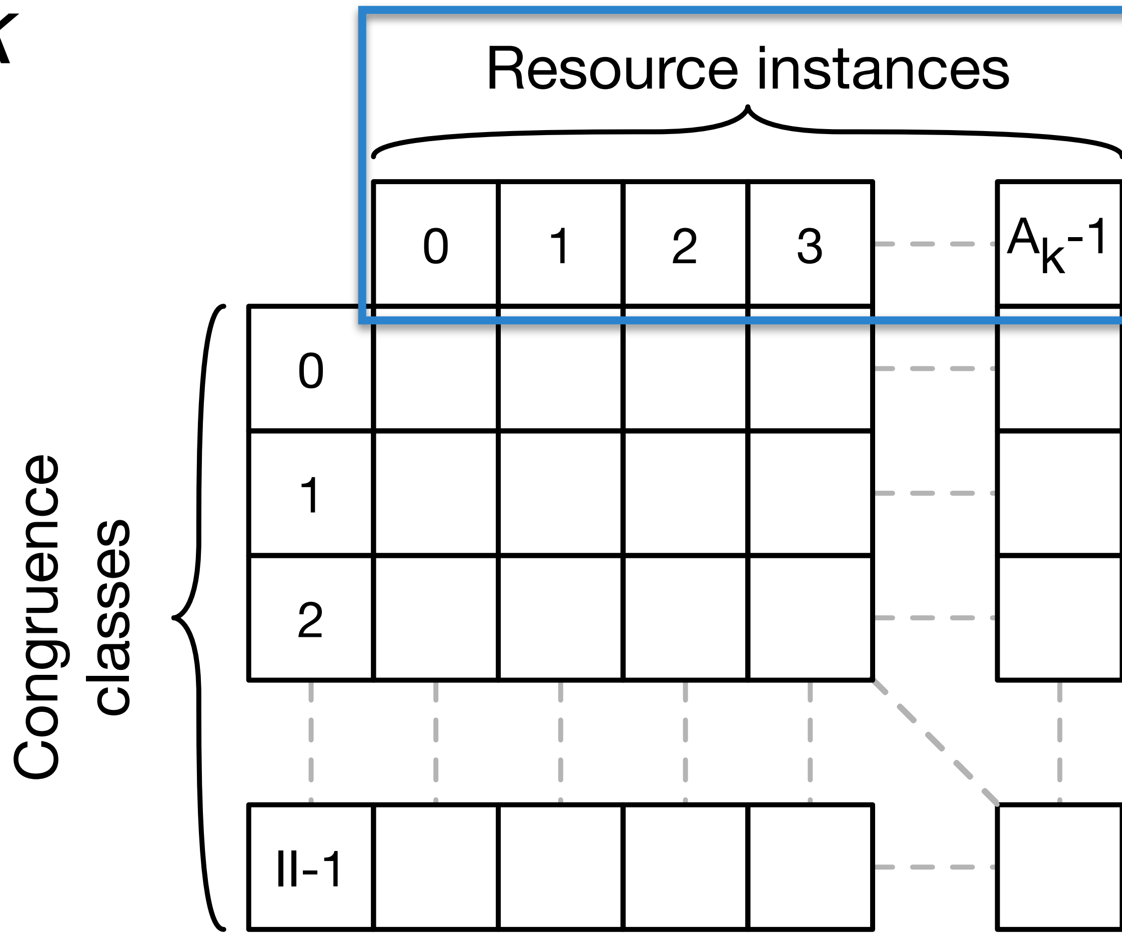
- Scheduling graphs with only typical HLS precedence constraints and backedges is **easy**
  - e.g. as a System of Difference Constraints (SDC), special ILP that can be solved in **polynomial** time
- Approaches differ in the modelling of resource constraints

General Approach

- A_k instances/units/… of a certain scarce resource kind k



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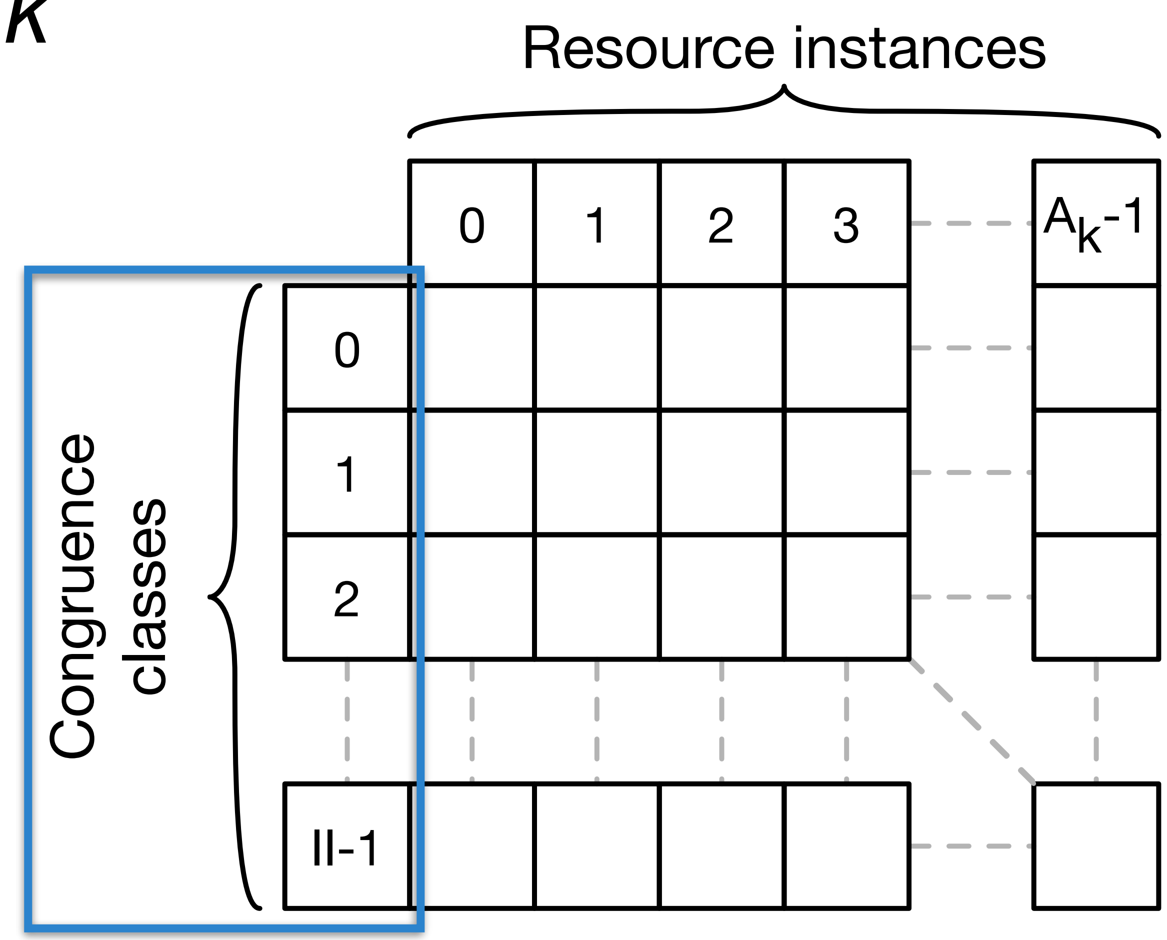

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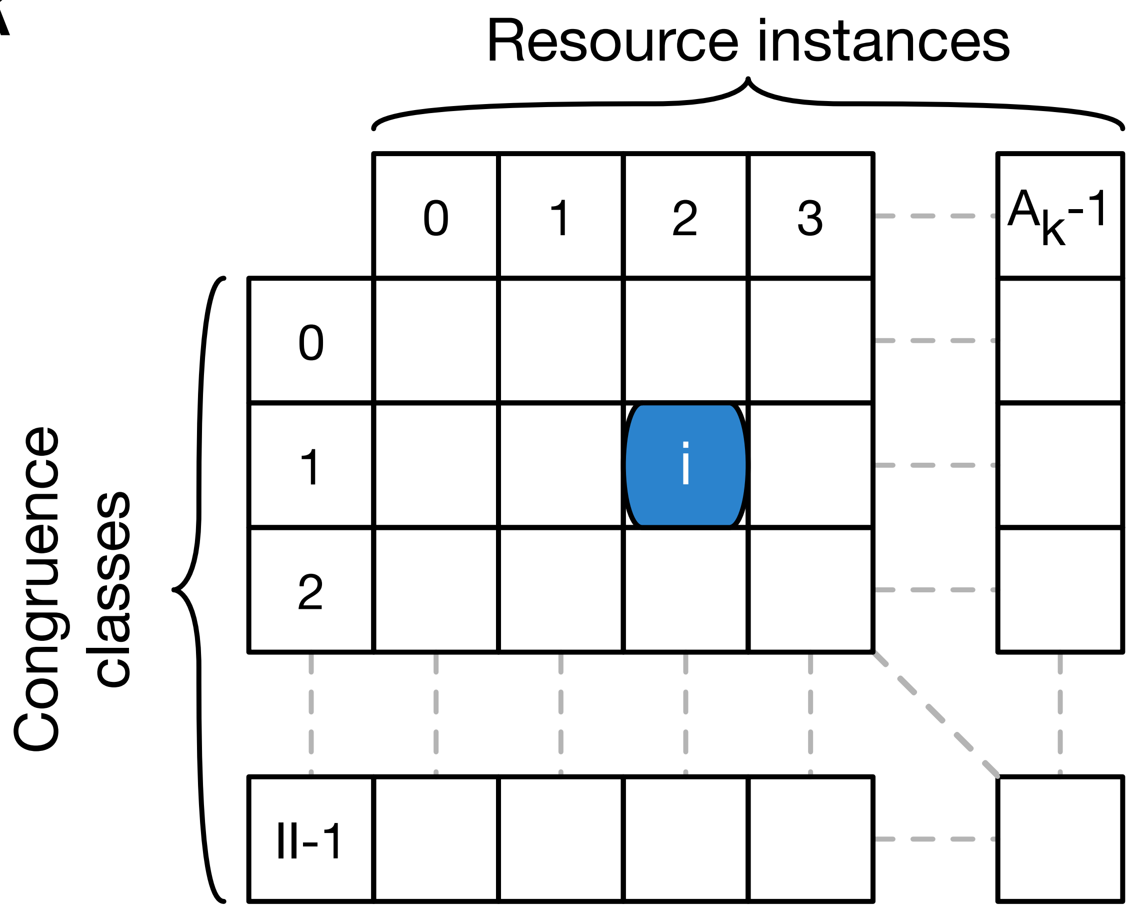

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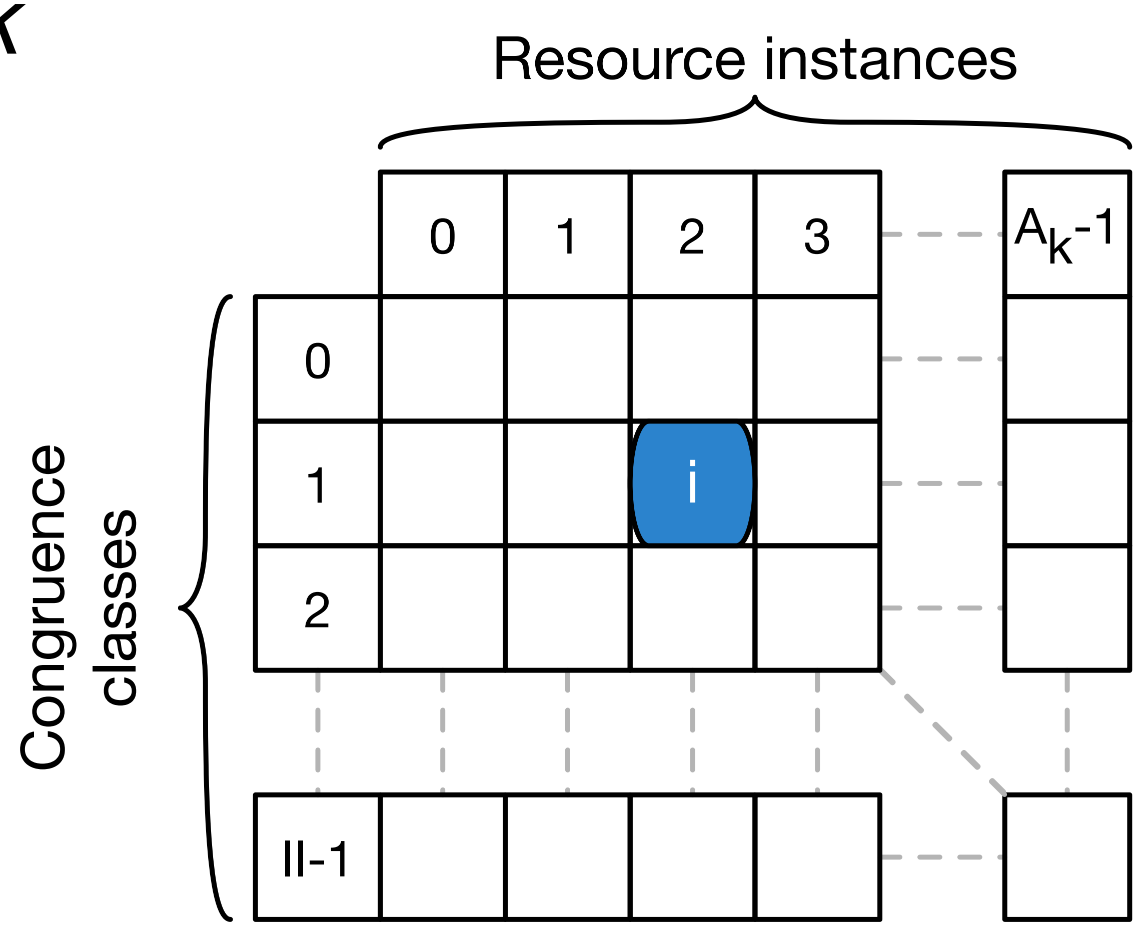
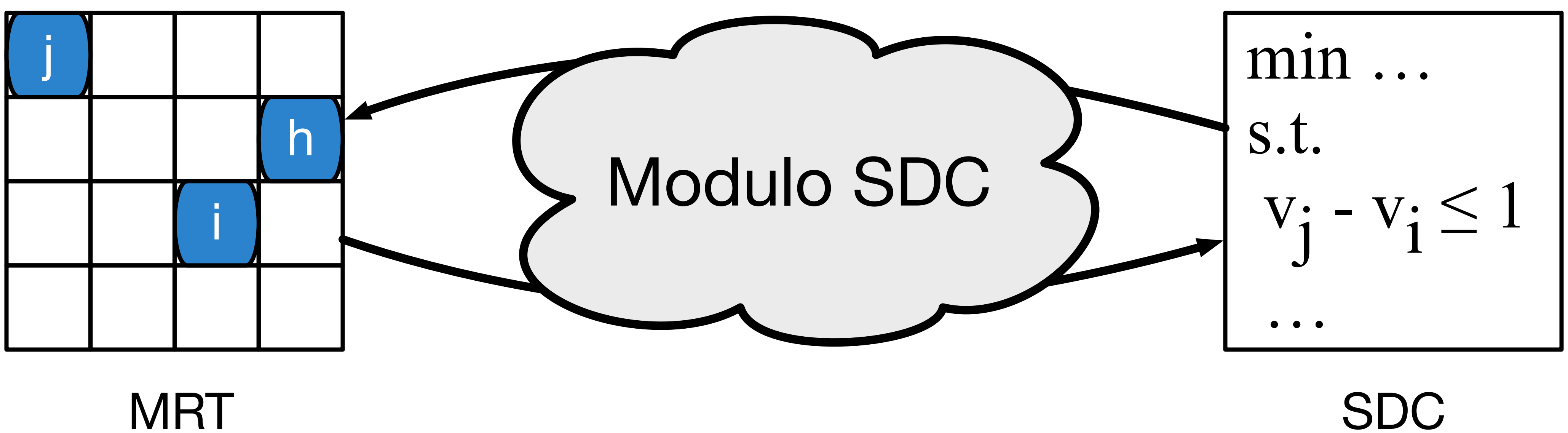
- *"modulo reservation table"* (MRT)



Modulo SDC

- **Heuristic** using an SDC and an explicit MRT



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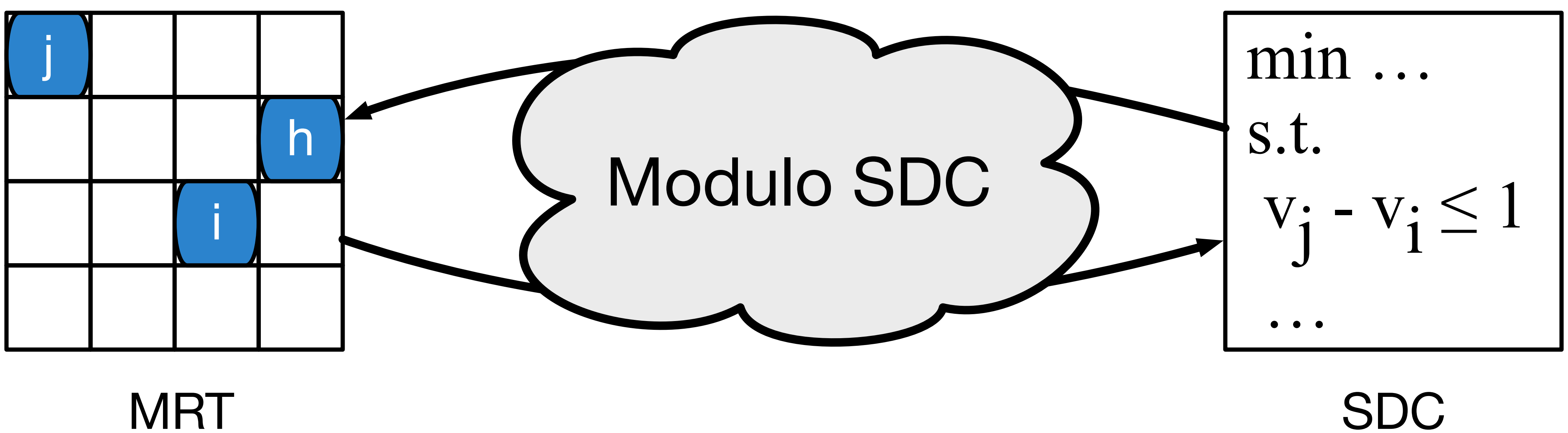

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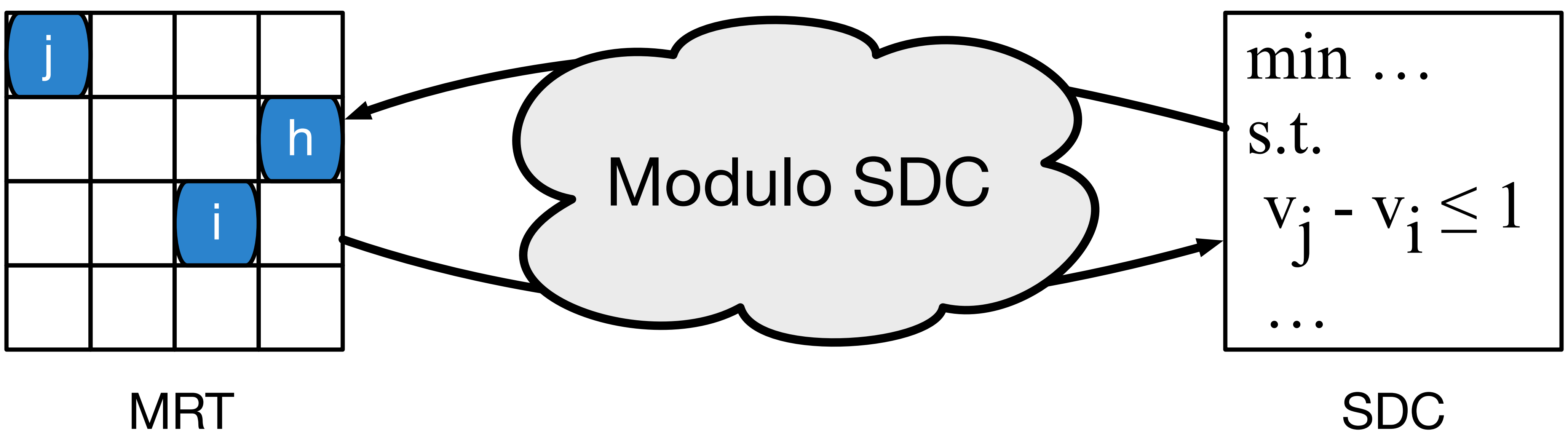

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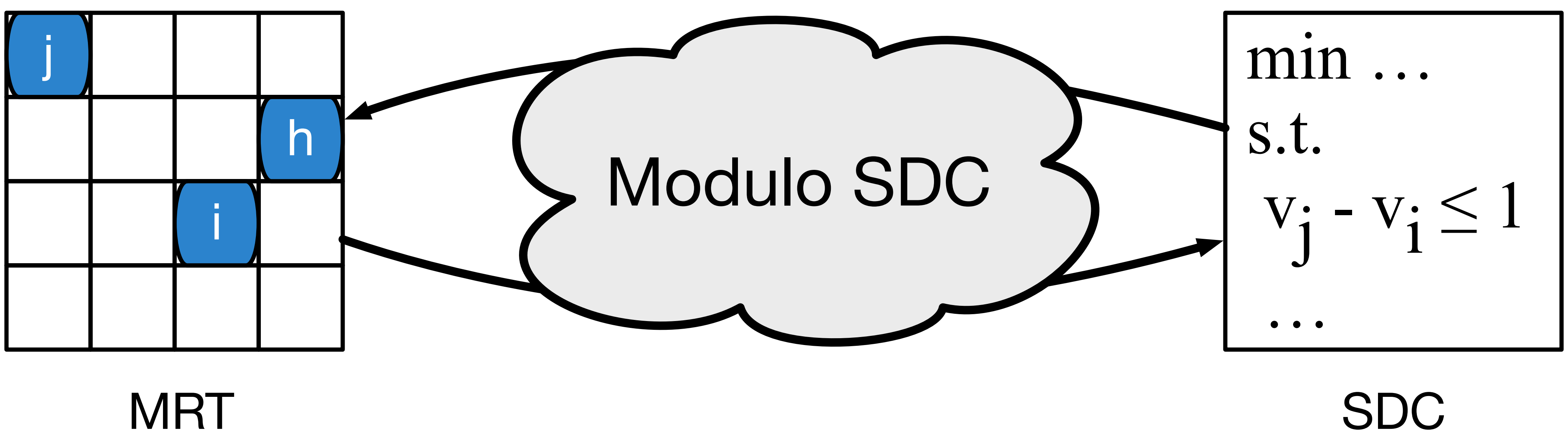

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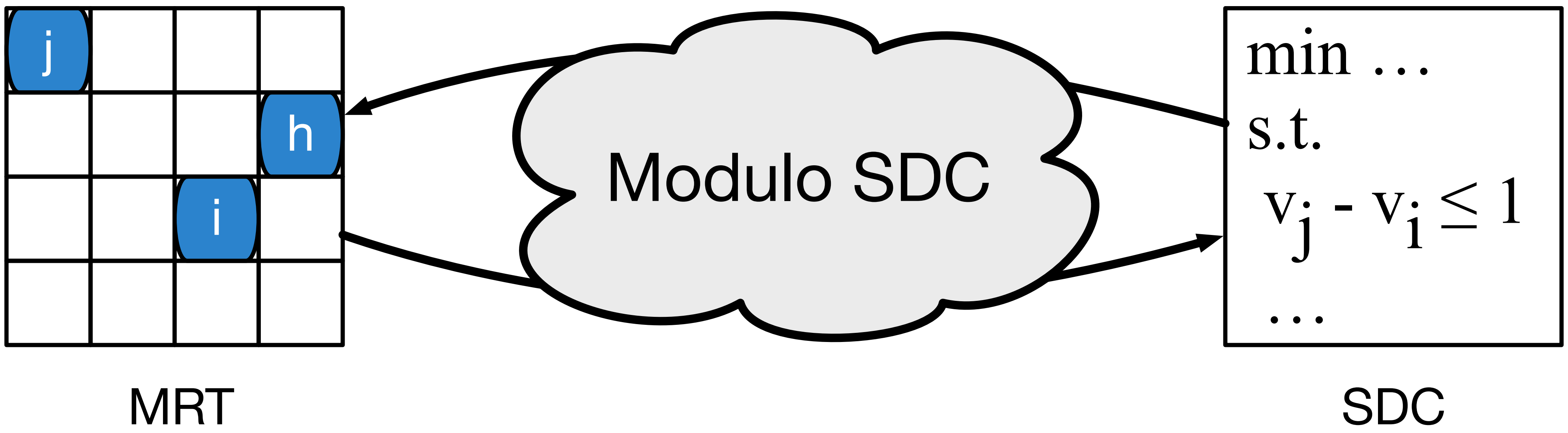
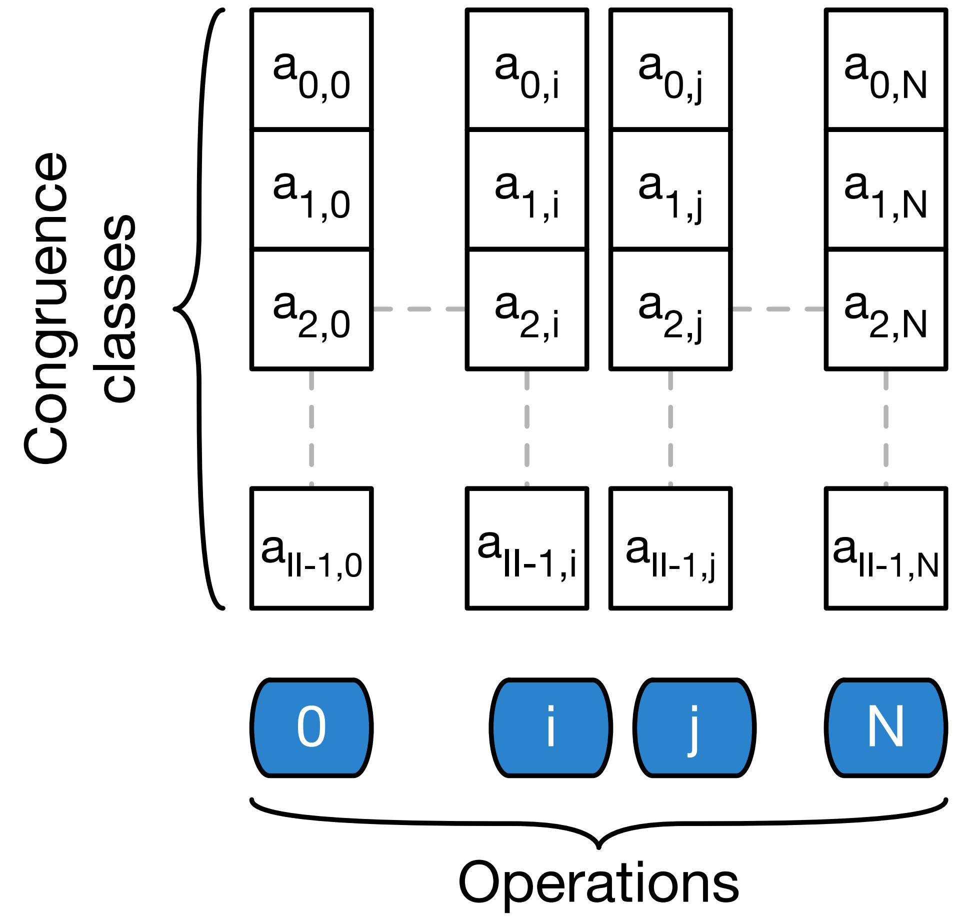
  - Successful if all resource-constrained ops fit in MRT



Eichenberger's Formulation

- **Exact** formulation
  general ILP with time-indexed binary variables
  $a_{m,i}$:= "operation i starts in congruence class m"



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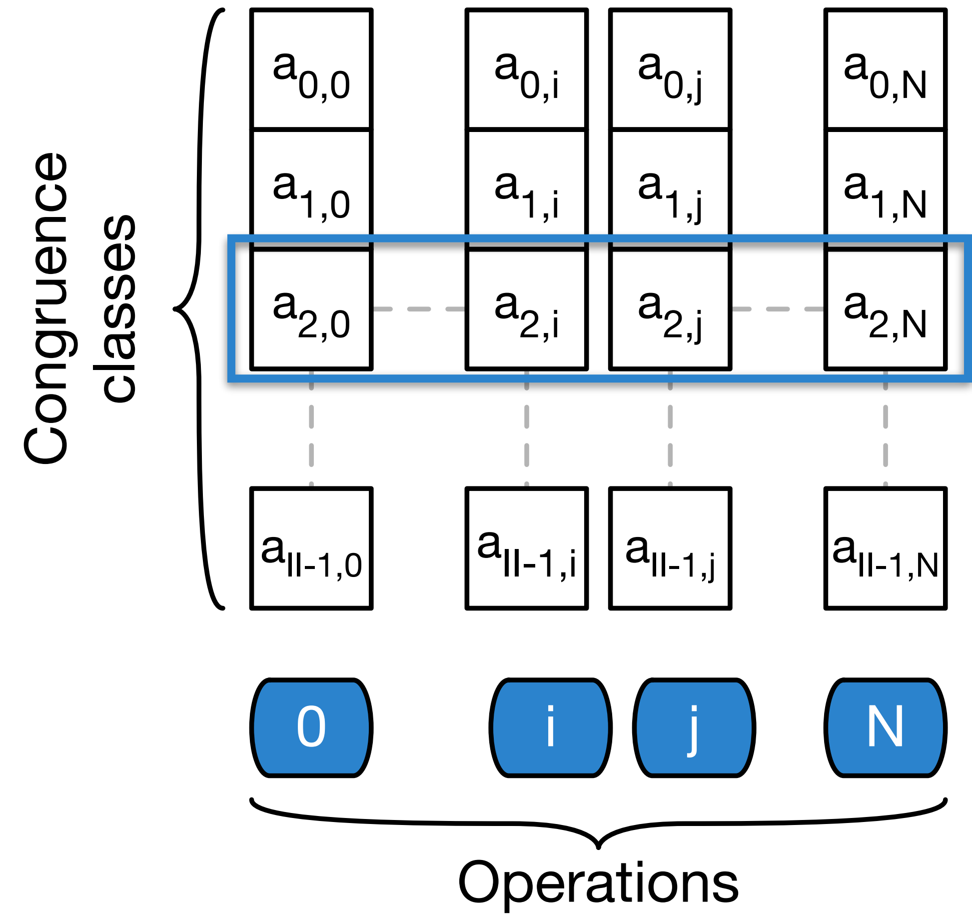
- Example: Resource constraint for
  kind *k*, congruence class 2
  fulfilled iff.

  $$\sum_x a_{2,x} \leq A_k$$

  for all operations *x* that use
  a *k*-resource



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- Moovac = **Mo**dulo **O**verlap **Va**riable **C**onstraints
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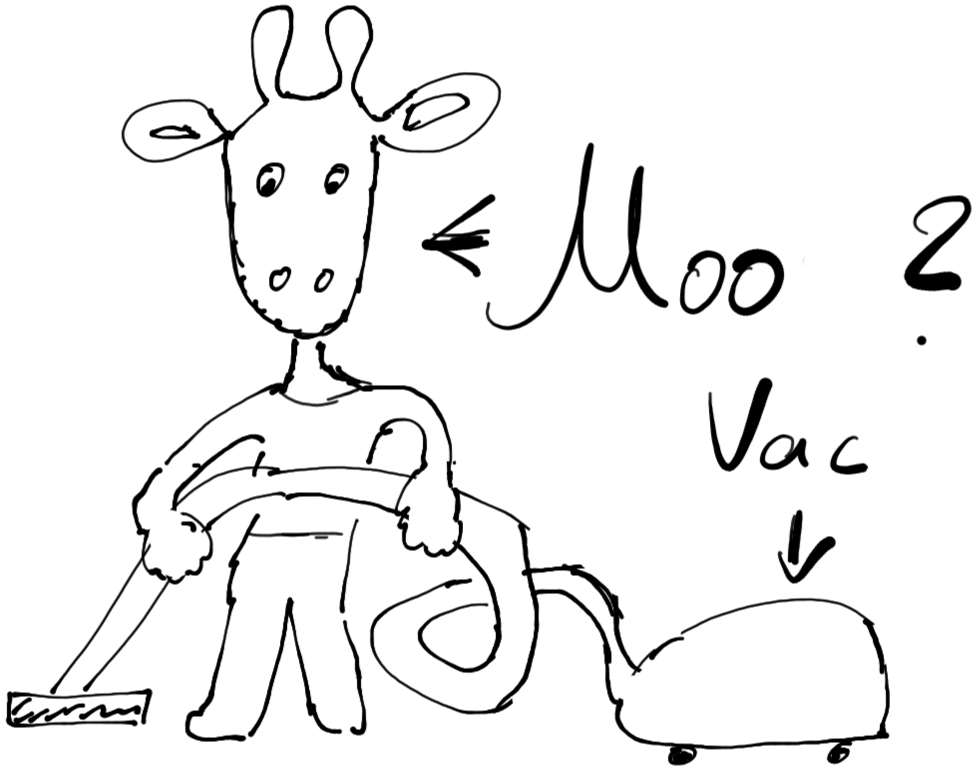

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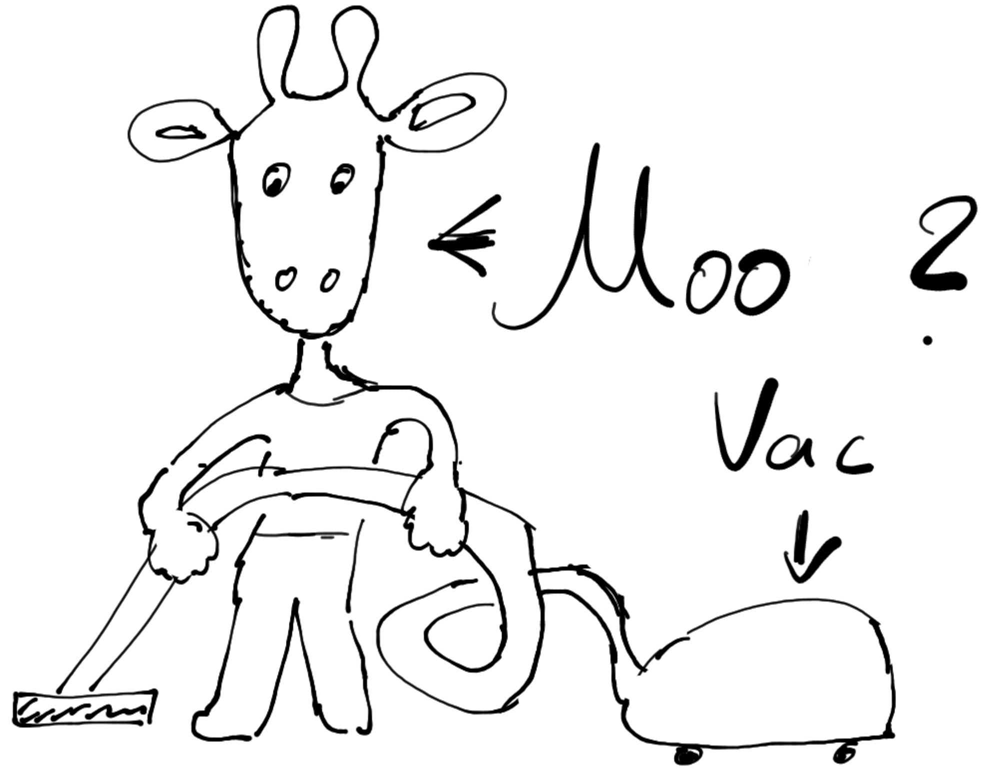

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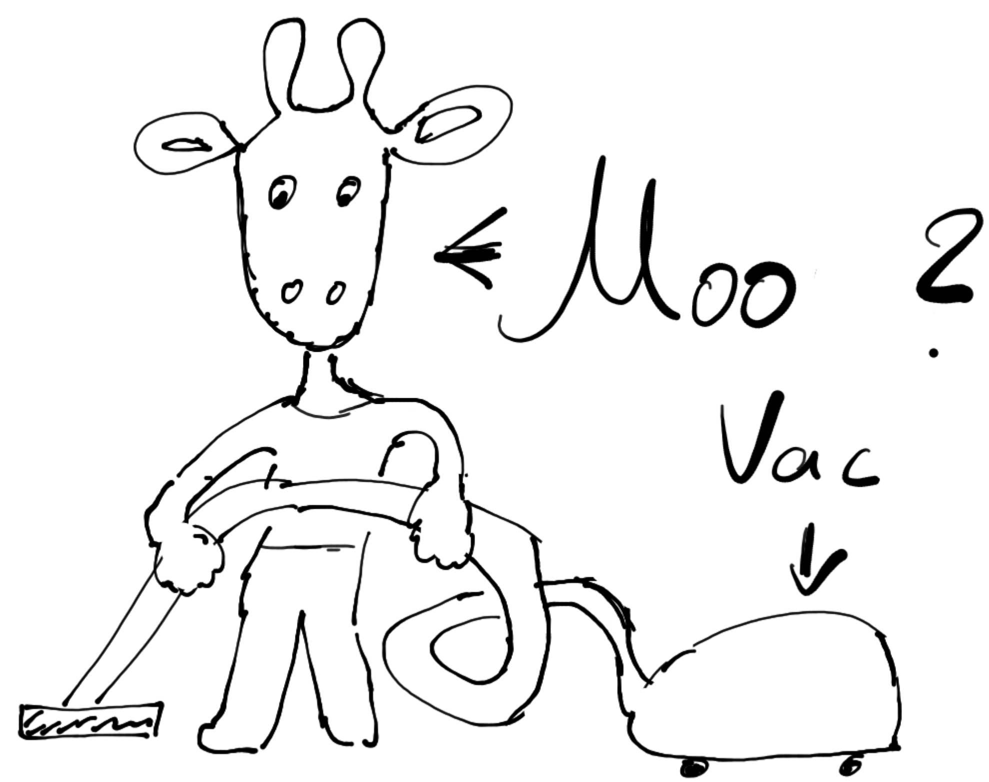

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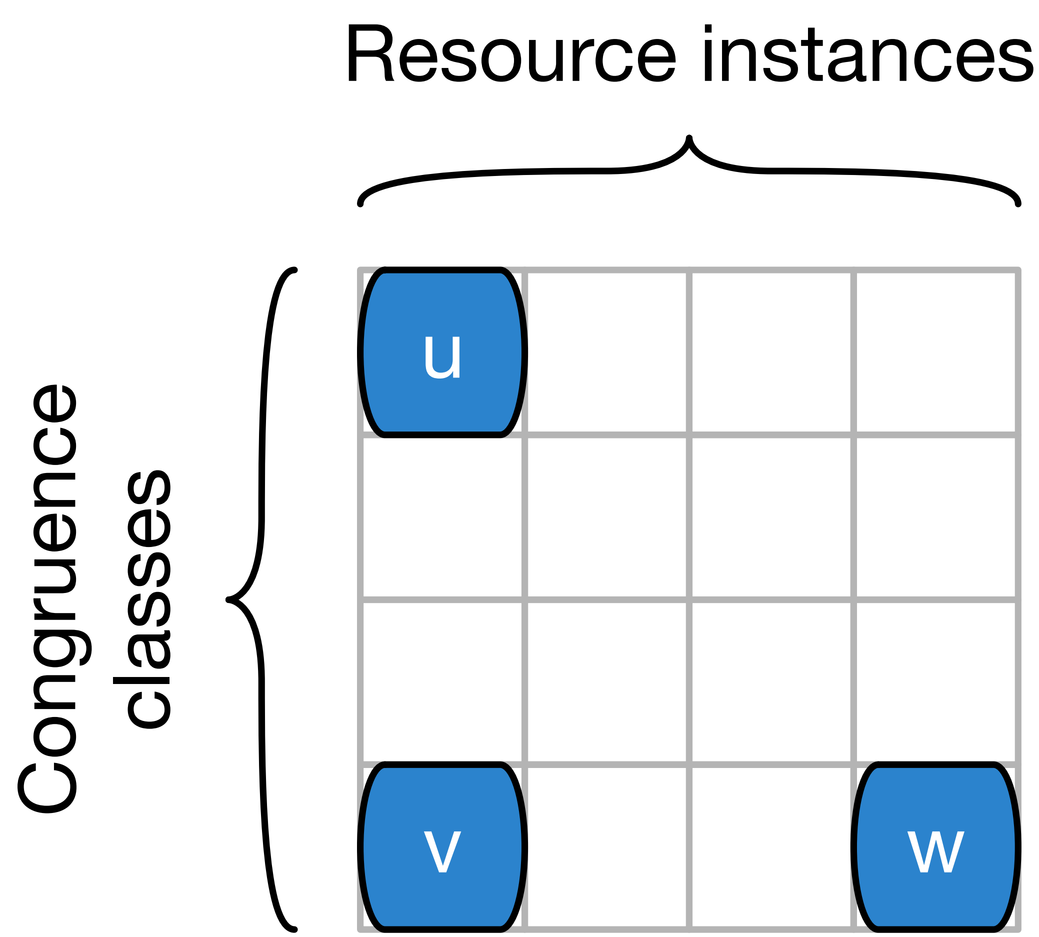
"i and j are either assigned to **different resource instances**, or scheduled to **different congruence classes**"

- No resource conflict iff.

$$\varepsilon_{ij} + \varepsilon_{ji} + \mu_{ij} + \mu_{ji} \geq 1$$

Moovac

- Tuples *(m_i, r_i)* ⇒ cell in MRT for operation *i*



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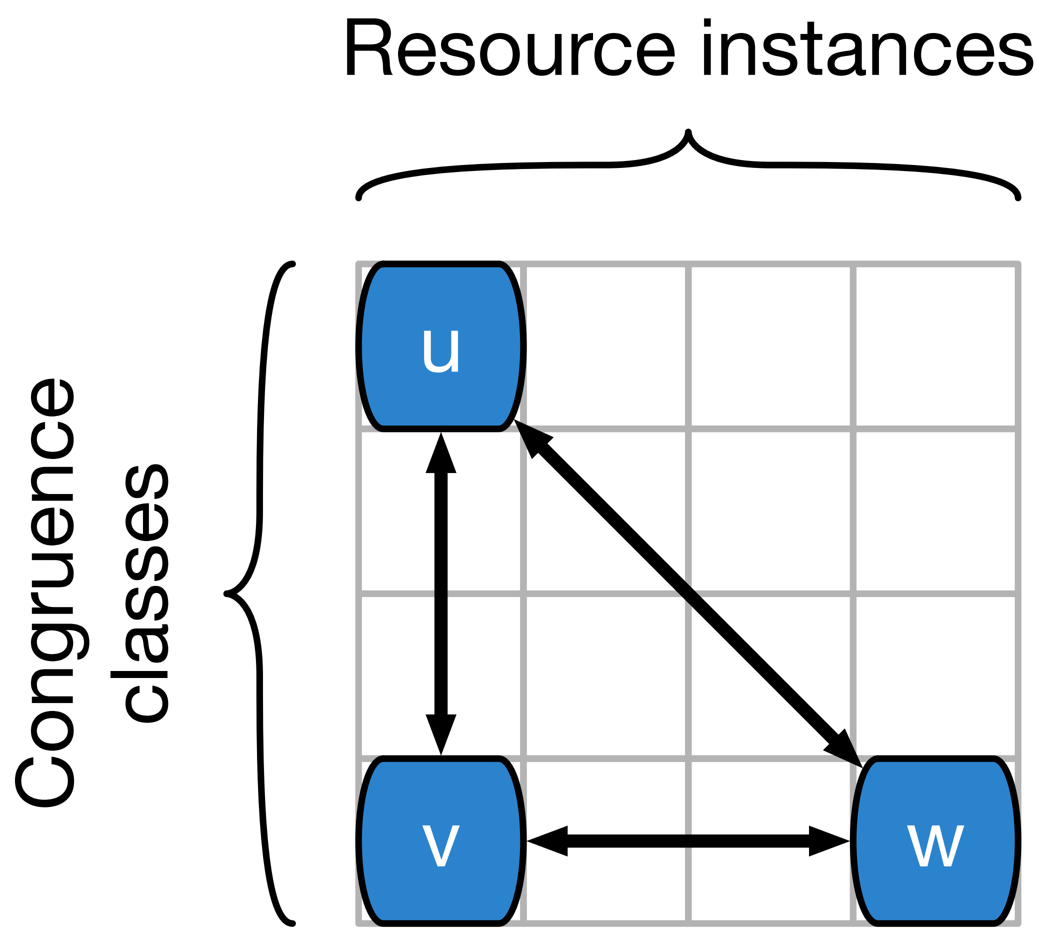

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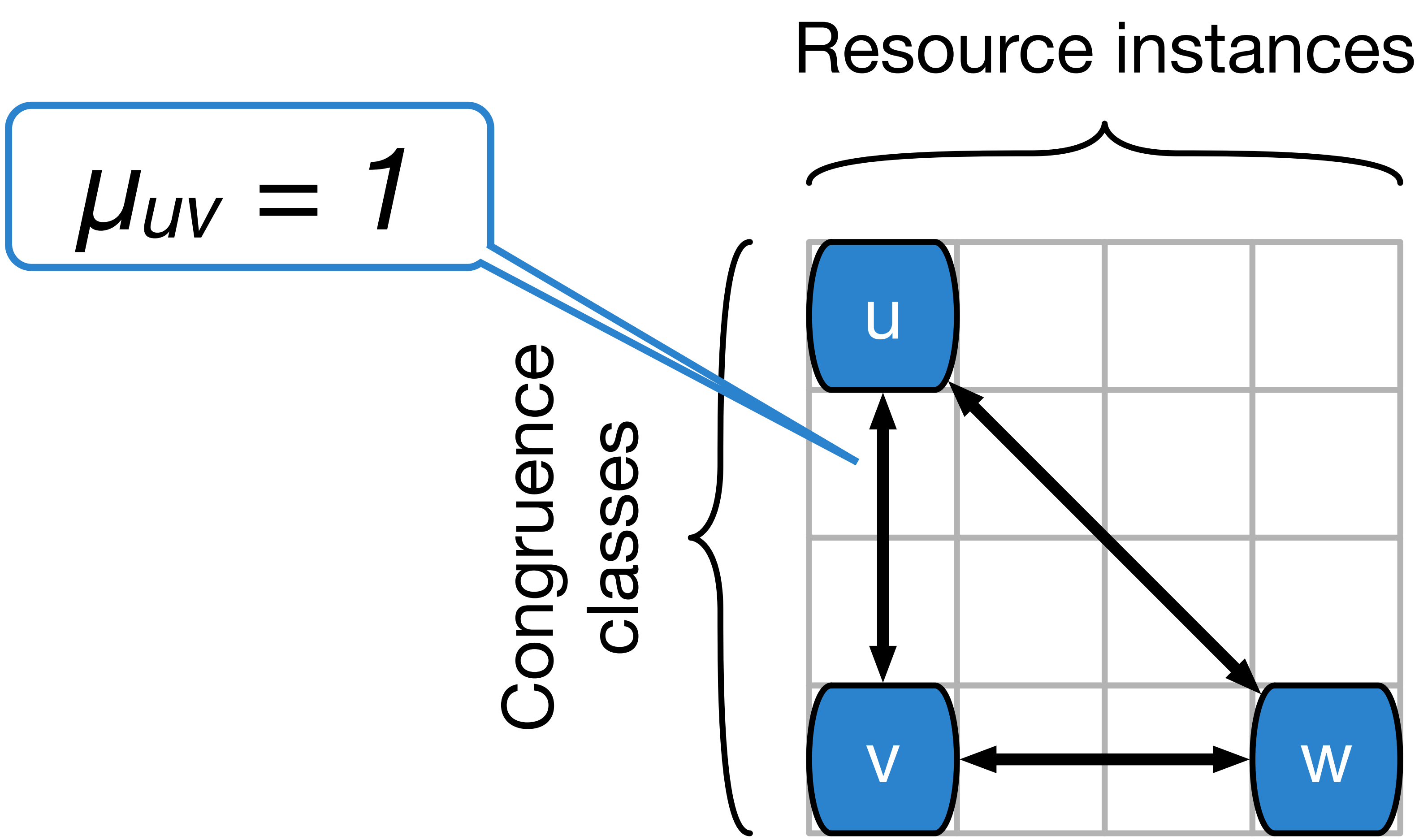

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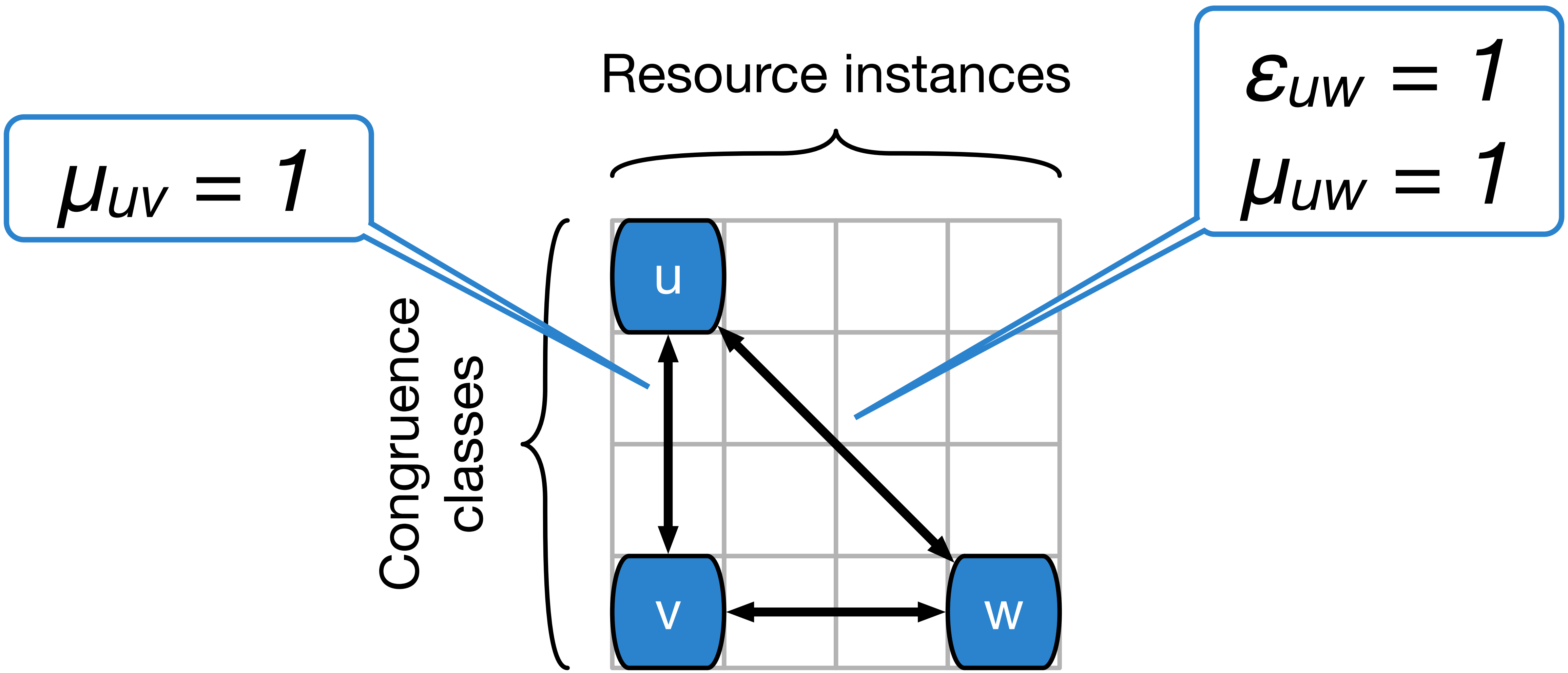

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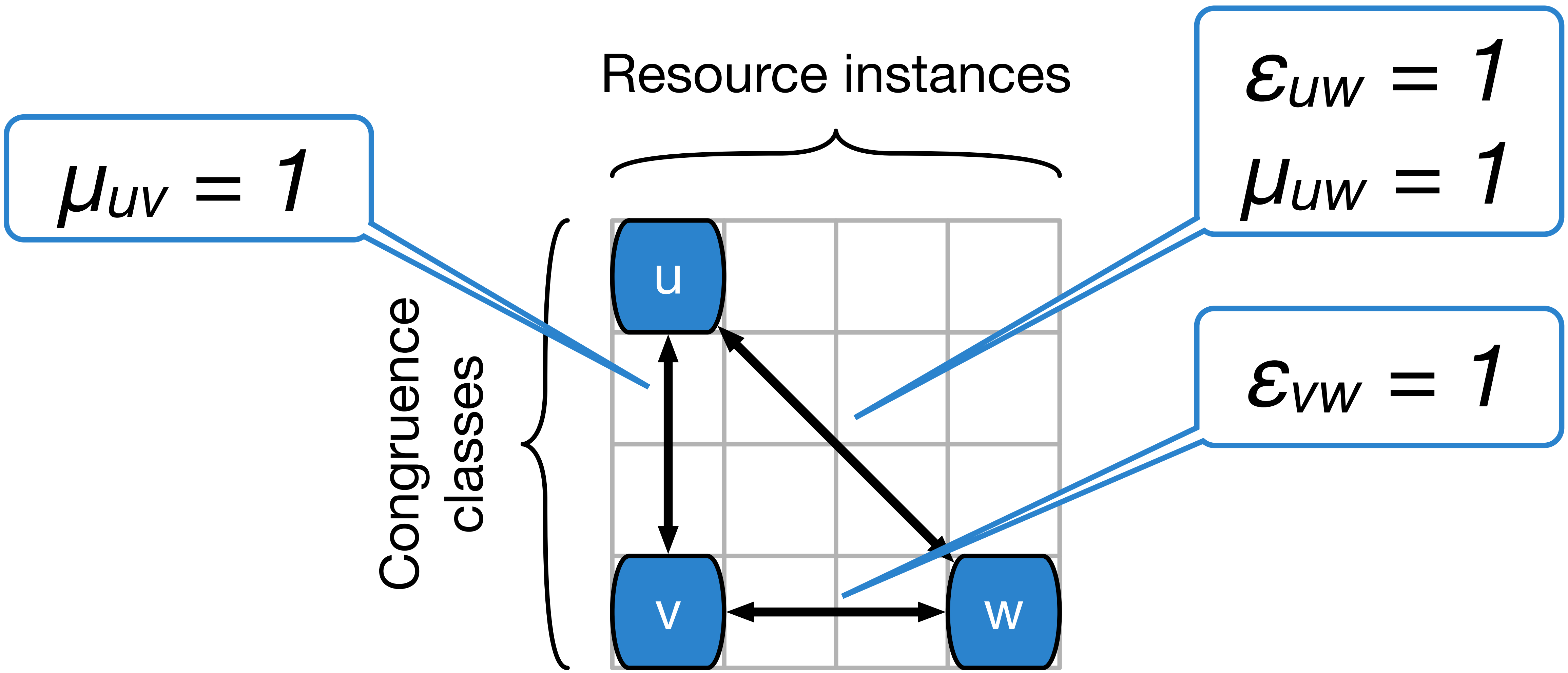

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Moovac
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- Novel **exact** formulation
- Uses fewer integer variables and overlap variables to model inequality between them

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- Attempted to schedule 225 graphs from CHStone and MachSuite
  - up to 1124 operations /
up to 107 resource-constrained operations

Results (Quality)

- 5 min time limit

Graphs		Moovac vs. Modulo SDC *shorter II found by …*			Moovac vs. Eichenberger's ILP *shorter II found by …*		
Size	*#*	*Moovac*	*Same*	*M. SDC*	*Moovac*	*Same*	*E.B.'s*
all	225	6	217	2	6	219	0
small	203	1	202	0	0	203	0
large	22	5	15	2	6	16	0

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Exact schedulers should find same II, but E.B. hit time limit

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The timeouts dominate the overall time e.g. 96 x 5 min = 480 min

Results (Time)

- Scheduling duration with 5 min time limit:

Graphs		Moovac		Modulo SDC		Eichenberger's ILP	
Size	*#*	*Time [min]*	*Timeouts*	*Time [min]*	*Timeouts*	*Time [min]*	*Timeouts*
all	225	489	96	753	148	932	177
small	203	3	0	131	26	5	0
large	22	486	96	623	122	927	177

Moovac is faster than the other approaches

The timeouts dominate the overall time e.g. 96 x 5 min = 480 min

M. SDC seems to get stuck even on small graphs

Insights

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  - ILP solver “sees” whole problem, can **prove** infeasibility of scheduling attempt (often: **fast**)
  - Heuristic can only fail to find a solution in the given time budget

Insights

- Modulo SDC and Moovac complement each other

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- "Synergistic scheduling"

Moovac:	489 min
Modulo SDC:	753 min
Combined:	**429 min**

Insights

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- What makes Moovac better suited for HLS modulo scheduling than Eichenberger's ILP?
  - Up to 1000+ operations, candidate IIs > 50 require humongous amounts of decision variables in time-indexed formulation
  - Majority of ops is unconstrained, only subject to precedence constraints and exempt from all MRT handling in Moovac

Outlook

- Smarter search through the (rather large) II space

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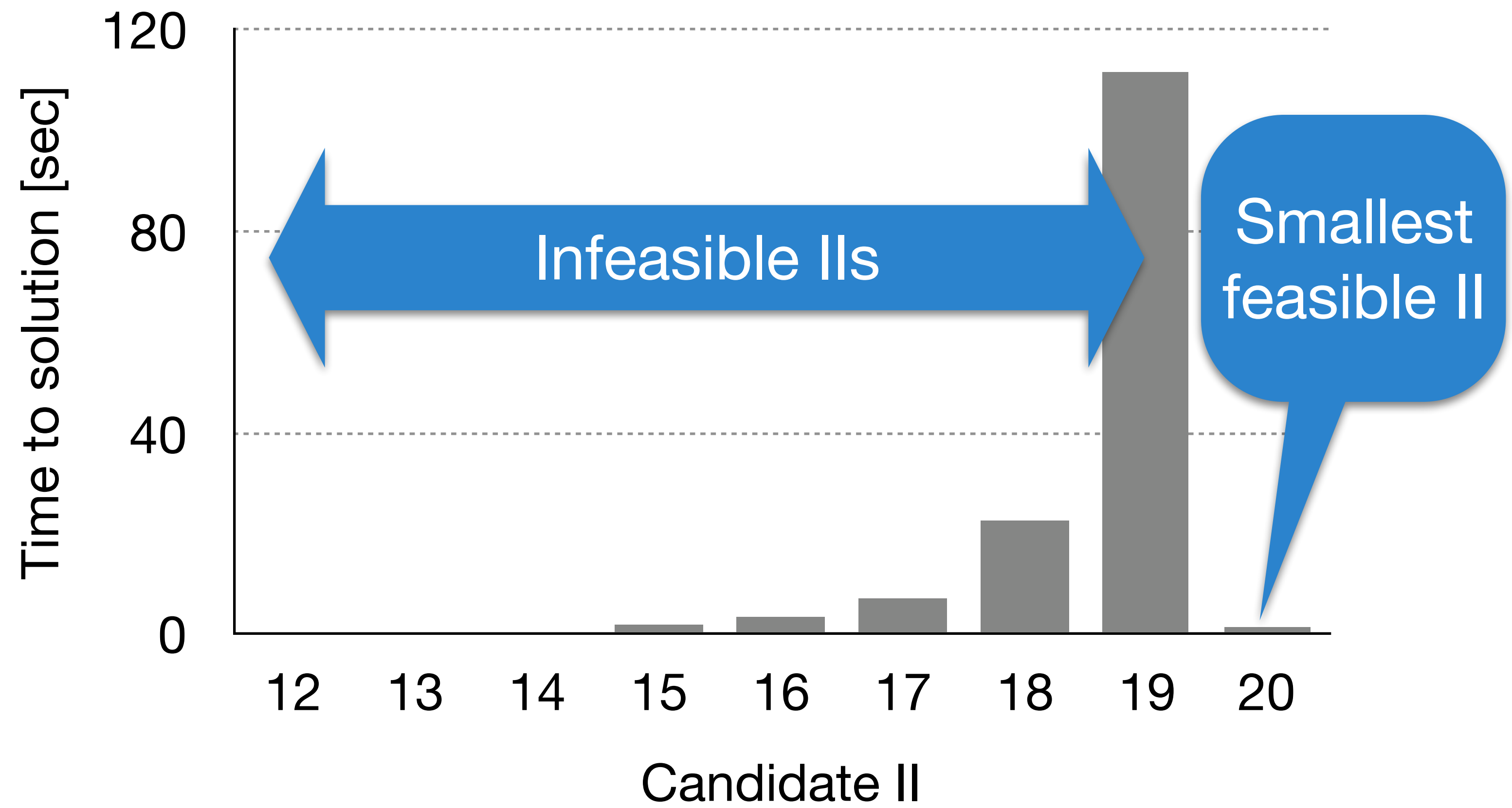
  - Observation:



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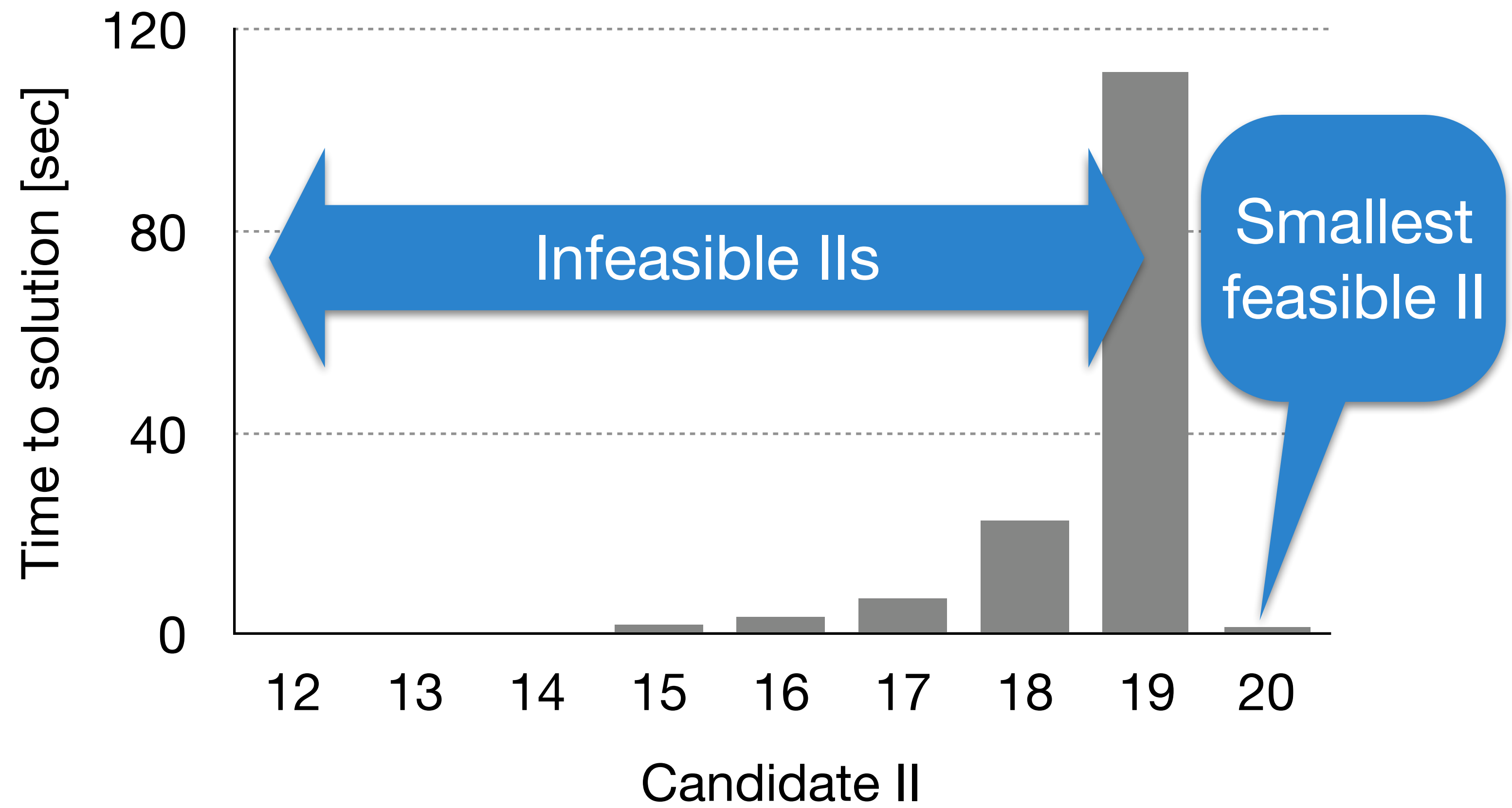
  - MaxII → MinII ?



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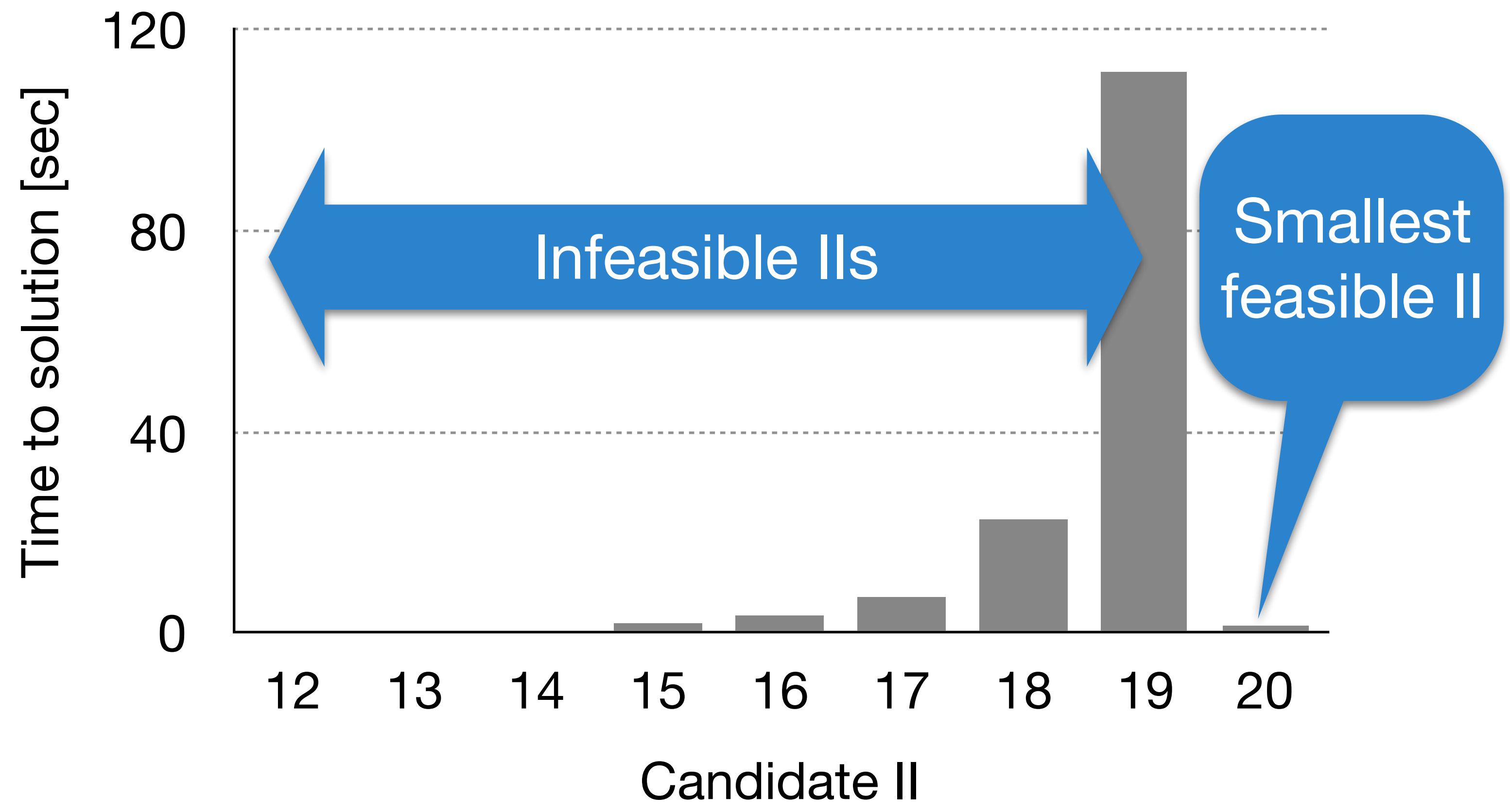

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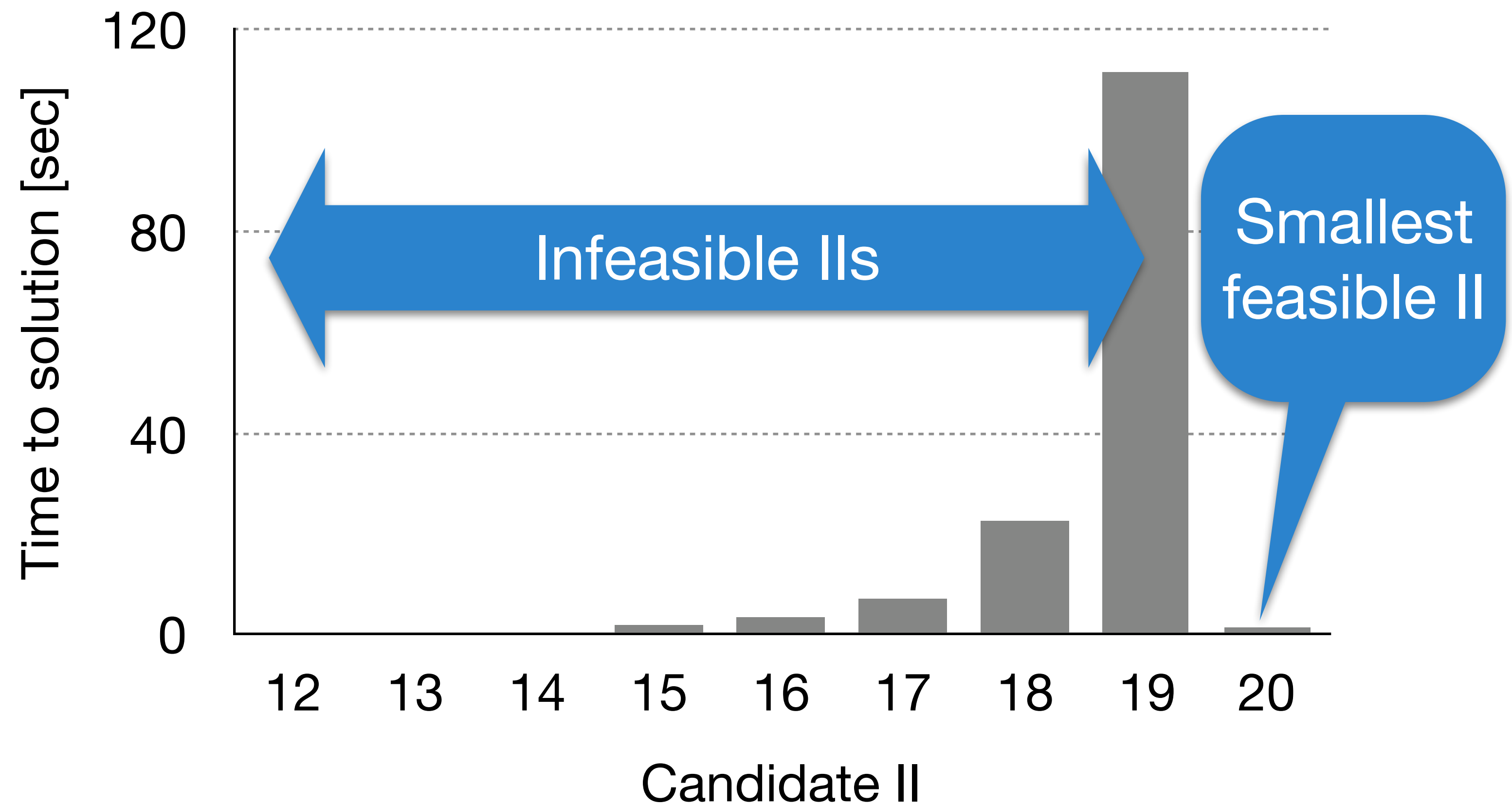

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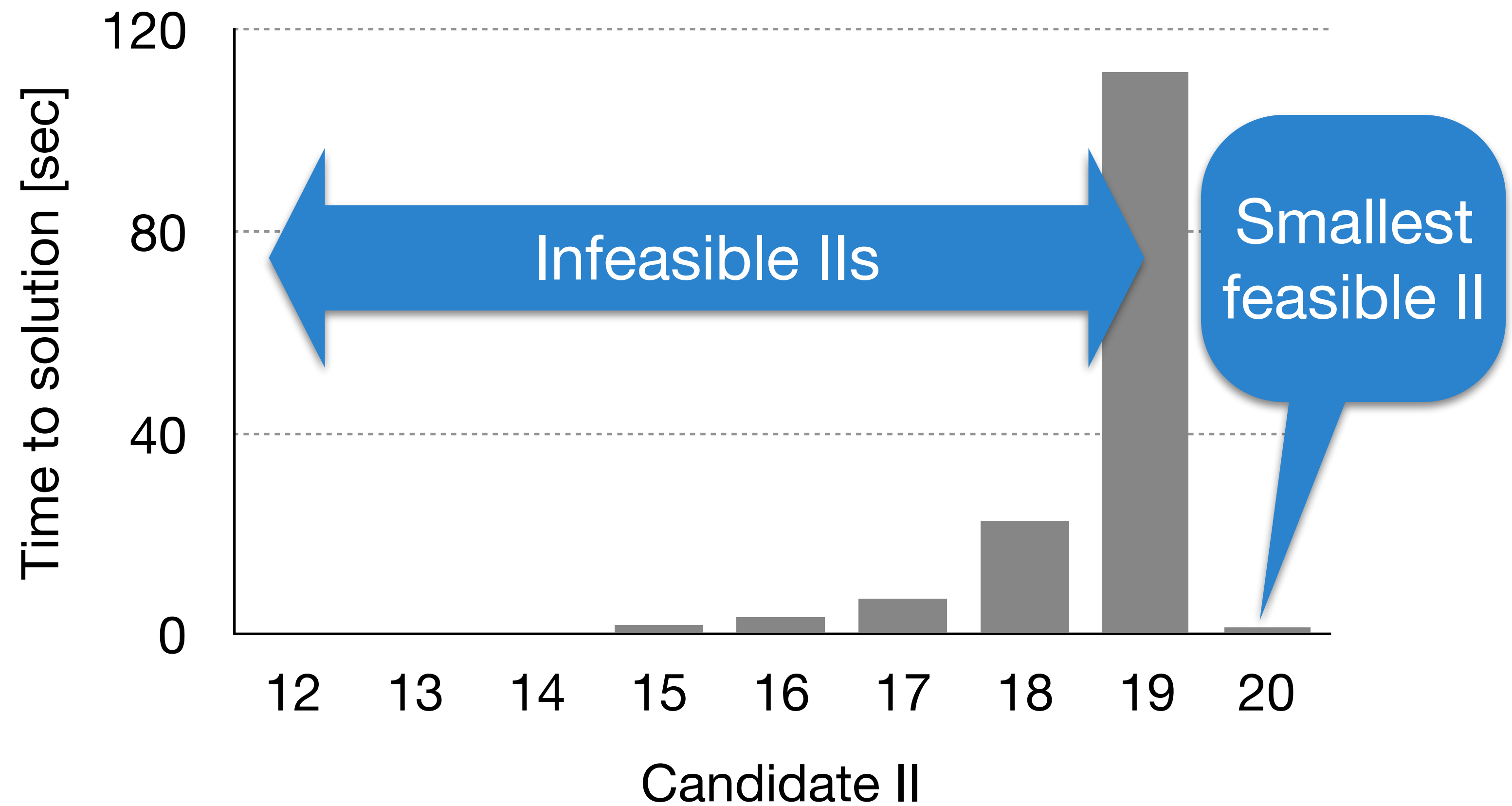

- Integrate II search into the Moovac formulation
  - Time-indexed formulations:
    # decision variables dependent on candidate II

Conclusion

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- Loop pipelining can reasonably be applied to wide range of HLS loops
- The Modulo SDC heuristic delivers results on a par with exact formulations
- The novel, exact Moovac formulation is surprisingly practical in its time-limited mode
- Diverse options to reduce the scheduling time even further exist

Thank you!

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