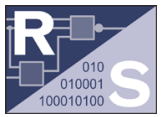
Towards Purposeful Design Space Exploration of Heterogeneous CGRAs: Clock Frequency Estimation



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Majored in Electrical Engineering and Information Technology and PhD candidate since end of 2015. Research associate with focus on CGRA hardware.

Prof. Christian Hochberger

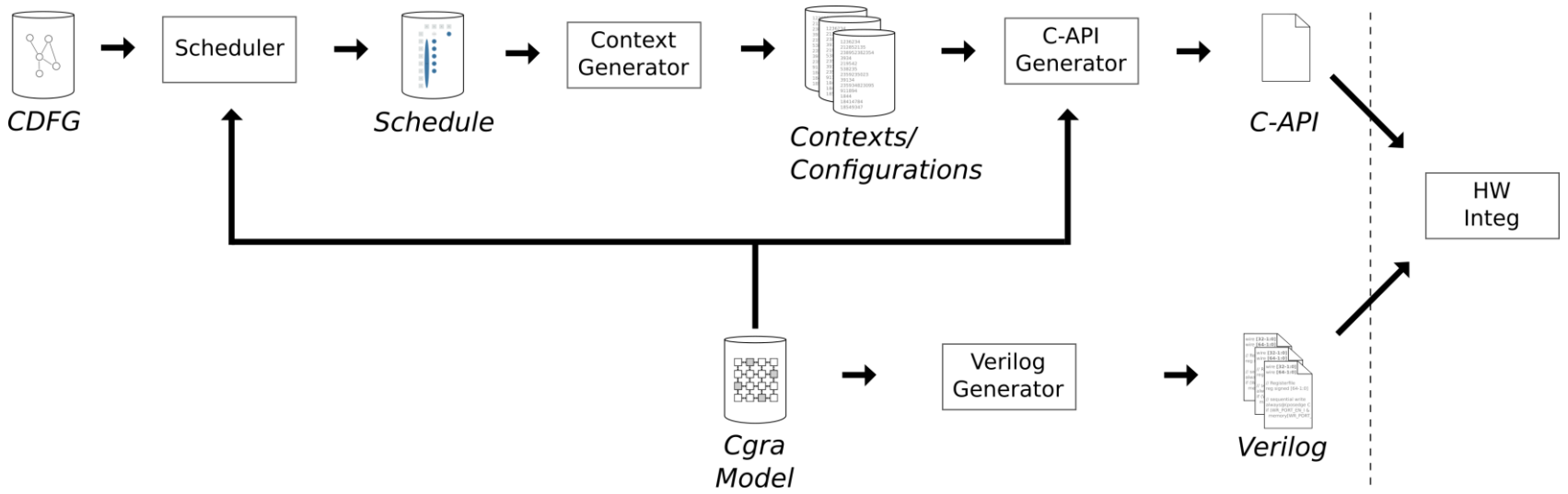
Chair for Computer Systems in EE department at TU Darmstadt since 2012. Before: Associate professor for embedded systems in CS department at TU Dresden since 2003. Diploma and PhD in computer science in 1992 and 1998.

M.Sc. Christoph Spang

Accomplished his master thesis at the Computer Systems group. Now a research associate at the Embedded Systems and Applications Group.

Micro-architecture & Automation

- Framework [1]:
  - CGRA Model
  - Scheduling
  - Verilog generator
  - Target: FPGA

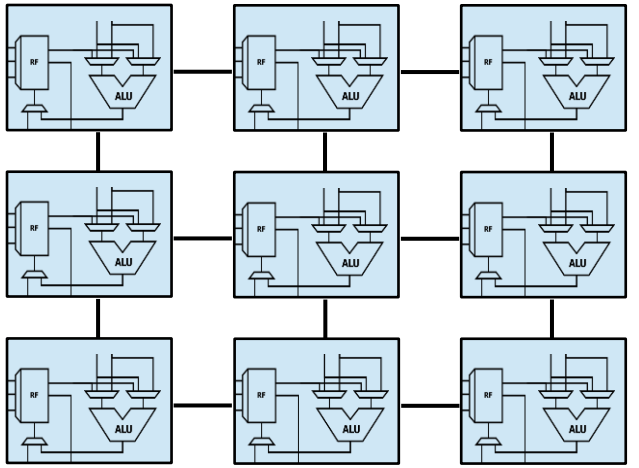


- Benefits:
  - Easy to modify and adjust
  - Free choice of CGRA composition/parameterization

[1] Wolf et al., “UltraSynth: Integration of a CGRA into a Control Engineering Environment“

Design Space Exploration

- Goal: Find optimal CGRA composition



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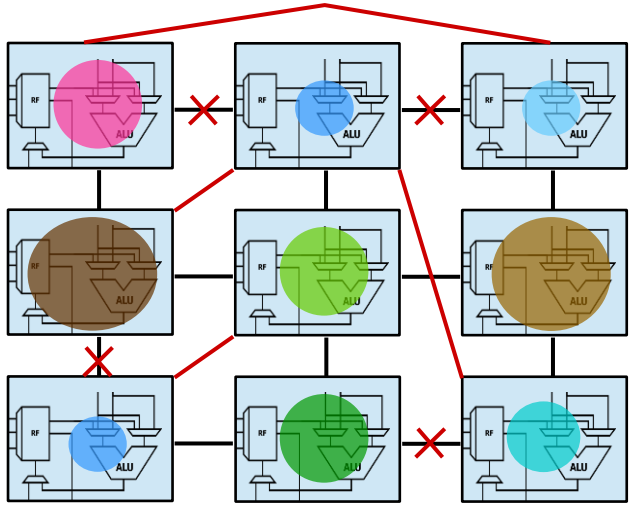

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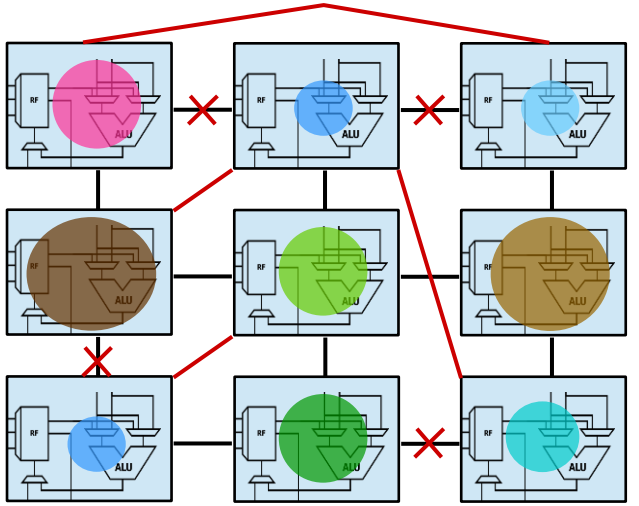


- Most promising DSE methodology: Simulated Annealing
  - Requires cost function → run-time of benchmarks
  - Synthesis infeasible → fast(!) estimation

State of the Art

- Heterogeneous designs: explicitly avoided [4]

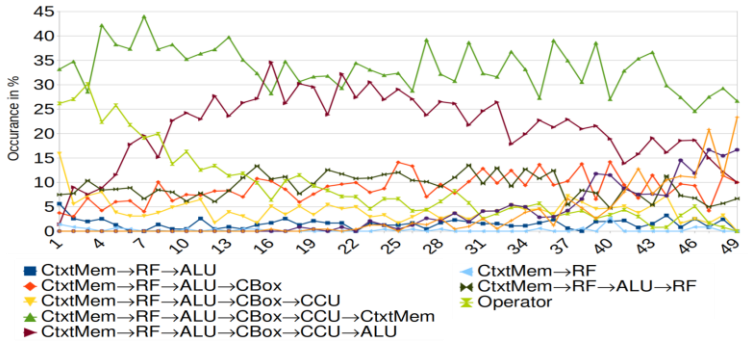
- Homogeneous: max error <50%, mean error <10% [2][3][6]
  - Well known implementation
  - Static timing analysis
  - Neural networks

Creation of Reference Set

- Systematical segmentation of design space
- Design space size = 1.21 x $\mathbf{10^{2596}}$
- Data base of **12.131** synthesized CGRAs

Analysis of Reference Set

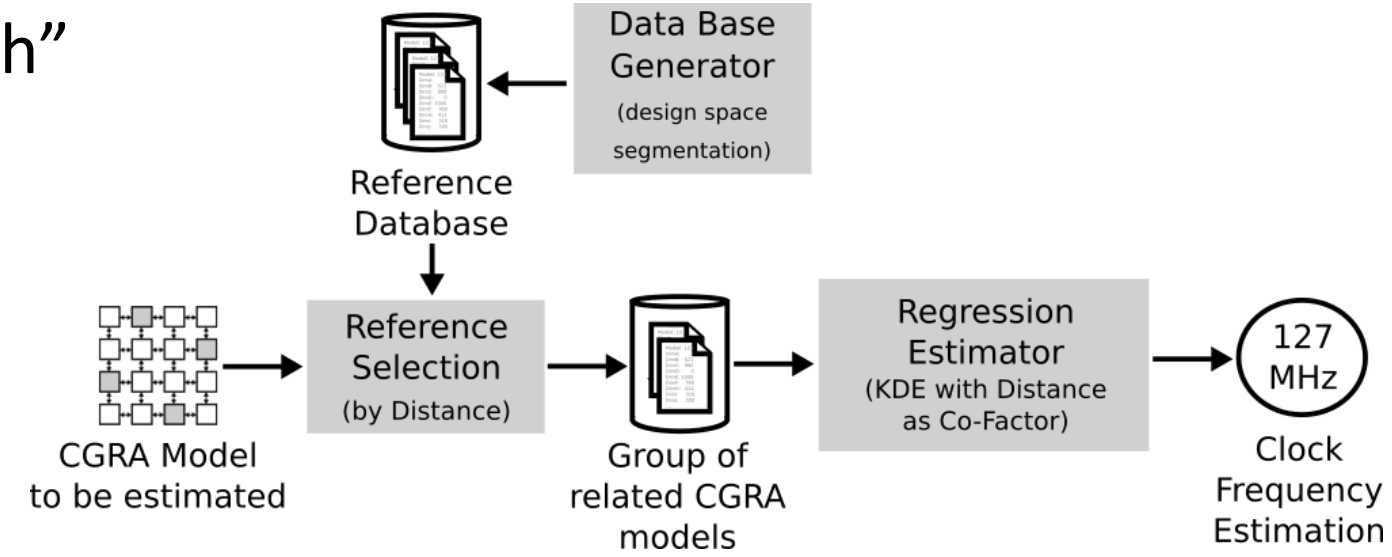
- 43 types of critical paths
- No clear correlation



- Analytical approach infeasible
- Initial ML approaches failed!

Statistical Estimator: Tool

- “Similar compositions should have a similar critical path”



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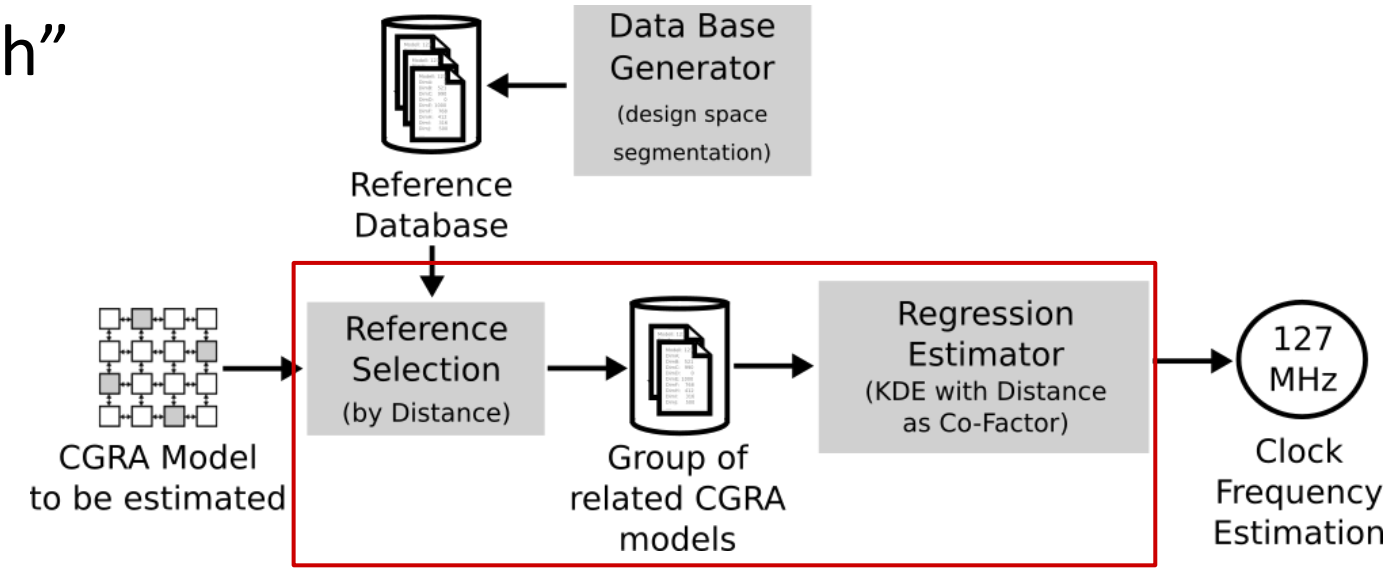
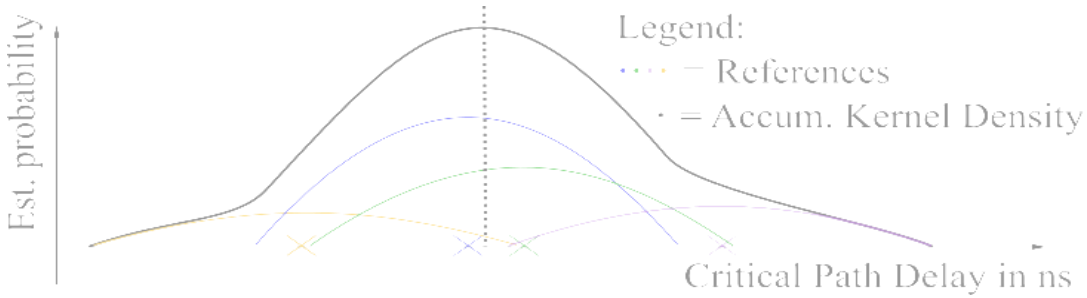


Statistical Estimator: Methodology

- Reference Selection
  - 10 closest CGRAs (empirical)
  - Determined by Euclid Distance

- # of interconnects	- max. # of PE inputs
- max # of estimated LUTs for a single PE	- standard dev. est. # LUTs per PE
- max RF size	- standard deviation RF sizes
- sum of RF sizes	- max context width
- standard dev. of context widths	- sum of context widths
- max Log Buffer size	- max OcmBuffer size
- size of Context Memory	- # PEs containing CF OPs
- empiric sum for specific CF path type	

- Kernel Density Estimation
  - Hann Curve over each delay
  - Weighted with the distance
  - Peak of the sum of all curves is the estimation



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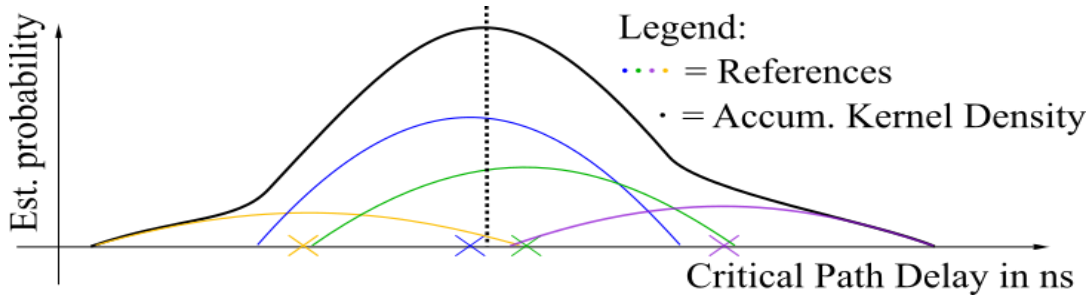
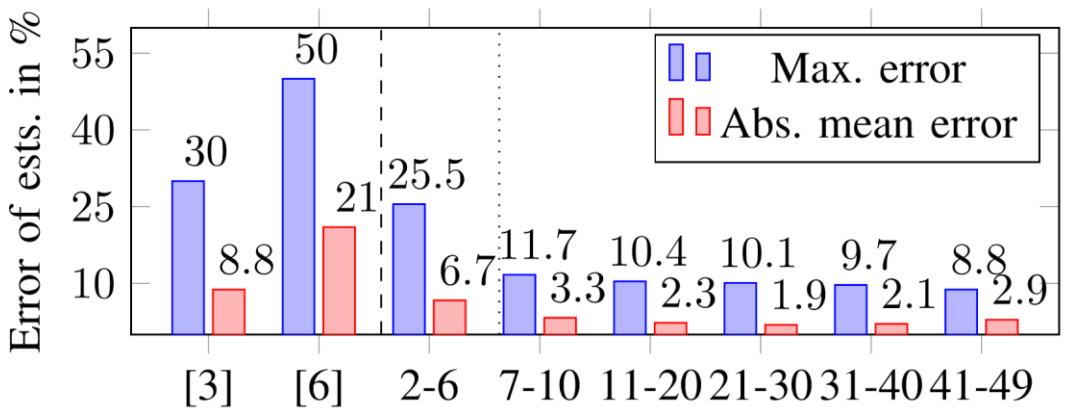
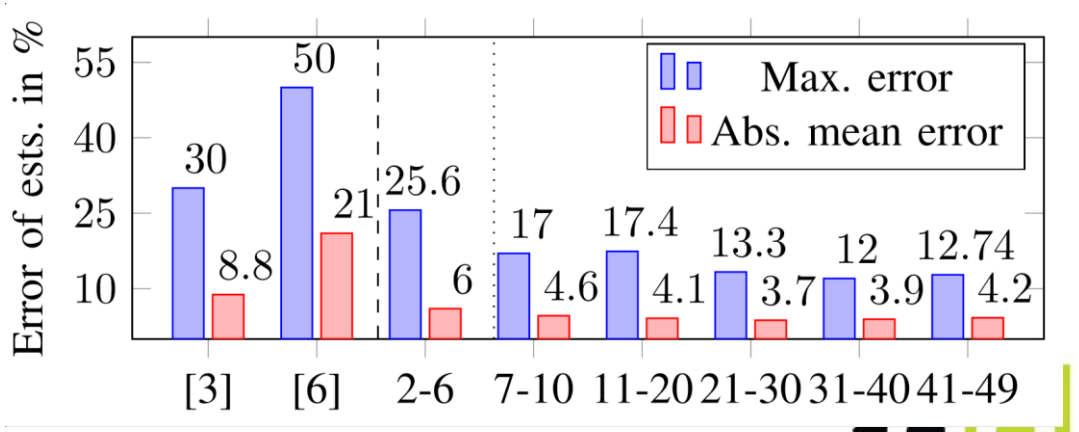


Evaluation: Accuracy

- Combinatorial branch selection
- References set: 7764
- Test set: 753



- Sequential branch selection
- References set: 3079
- Test set: 501



[3] Yan et al., “Area and Delay Estimation (...) of Coarse-grained Reconfigurable Architectures”

[6] Chen et al., “High-Level Power Estimation and Low-Power Design Space Exploration for FPGAs”

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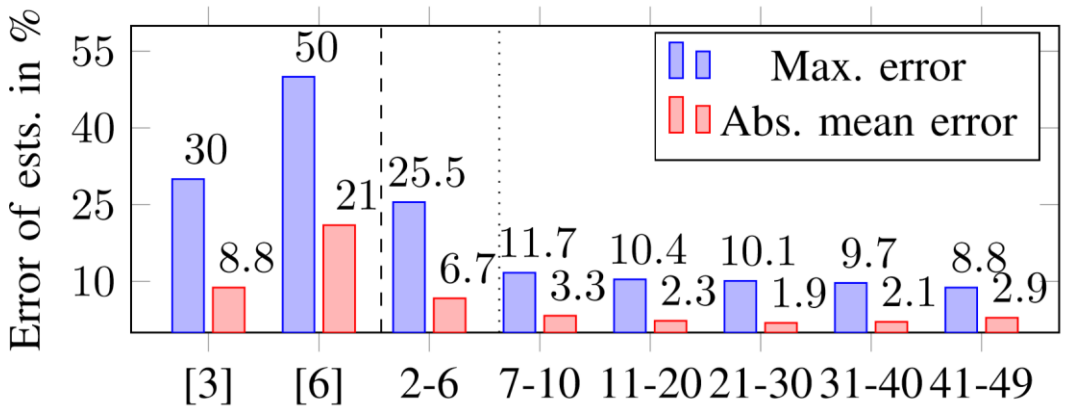

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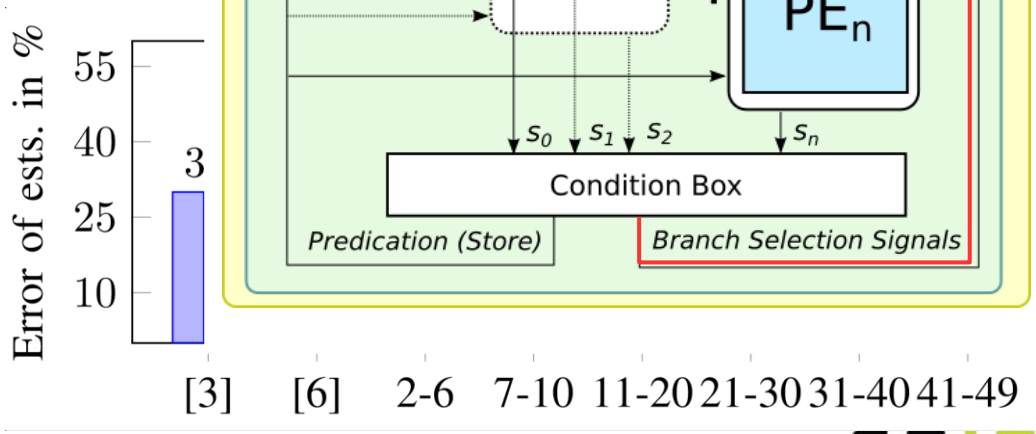

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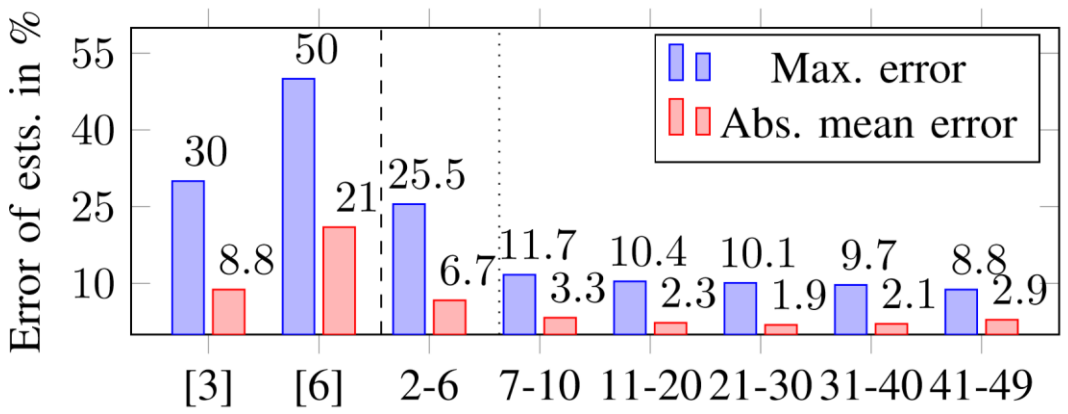

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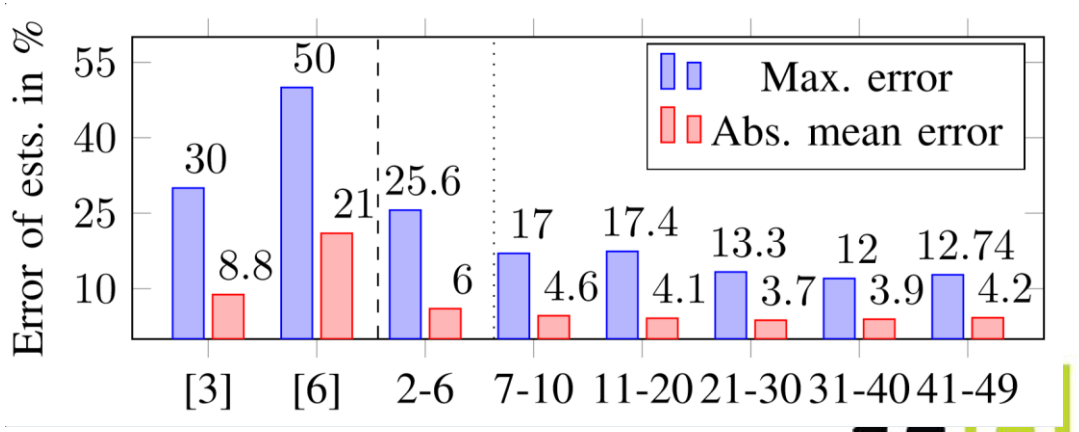

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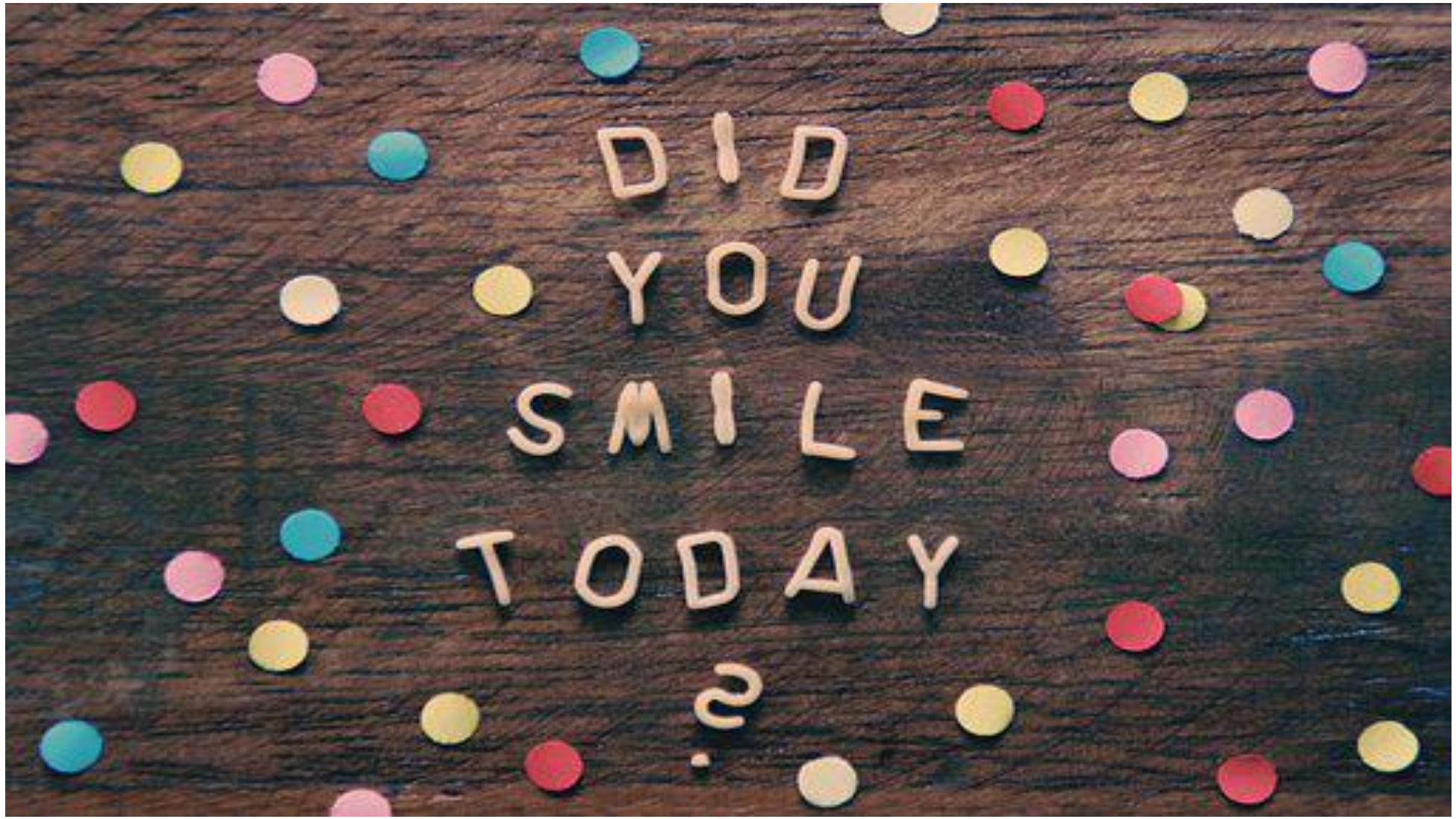
Conclusion

- Clock frequency estimation of heterogeneous and irregular CGRAs is highly challenging.

- **Statistical estimation** with a **mean error of 1.9-4.6%** and a **maximum error below 17.4%**.

- Run-time per estimation: 17.26 ms – 85.33 ms.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