High-Level Synthesis of Portable Custom Instruction Set Extensions for RISC-V Processors from Descriptions in the Open-Source CoreDSL Language

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Introduction

- Modern embedded, IoT devices are expected to run ML, signal processing, etc.
- ISA extensions ("ISAX") → cost-effective + energy-efficient way to accelerate applications on generic base cores
- RISC-V ecosystem: 0º for ISAX approach
- But in practice: only limited reuse and exploration
  - Implementing an extension manually: hard
  - Existing solutions are vendor-specific, not portable across cores or microarchitectures

Idea: Accessible and portable ISAX design

- **Longnail**: Microarchitecture-agnostic high-level synthesis
  - CoreDSL: new user-friendly language
  - Bi-directional communication with SCAIE-V interface generator
  - Automatic integration into base core

ISAXes beyond R-type instructions

- Two novel language constructs in CoreDSL:
  - always-block: Execute behavior continuously, independently of fetched instructions
  - spawn-block: Other instructions can be executed in parallel to spawned behavior
- Extended SCAIE-V tool provides interface to the core
  - handles data hazards and arbitration, provides access to program counter, instantiates custom registers

CoreDSL — new ISAX design language

- Intuitive ADL with C-inspired syntax & concise structure
- Bitwidth-aware type system to prevent implicit loss of precision
- Control-flow constructs & ISAX-specific syntax extensions

Impact in Scale4Edge ecosystem

- CoreDSL successfully used by application engineers to accelerate audio event detection application
- Successful tapeout with earlier version of SCAIE-V and handwritten ISAX module → 15 % area for ISAX enables real-time performance

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